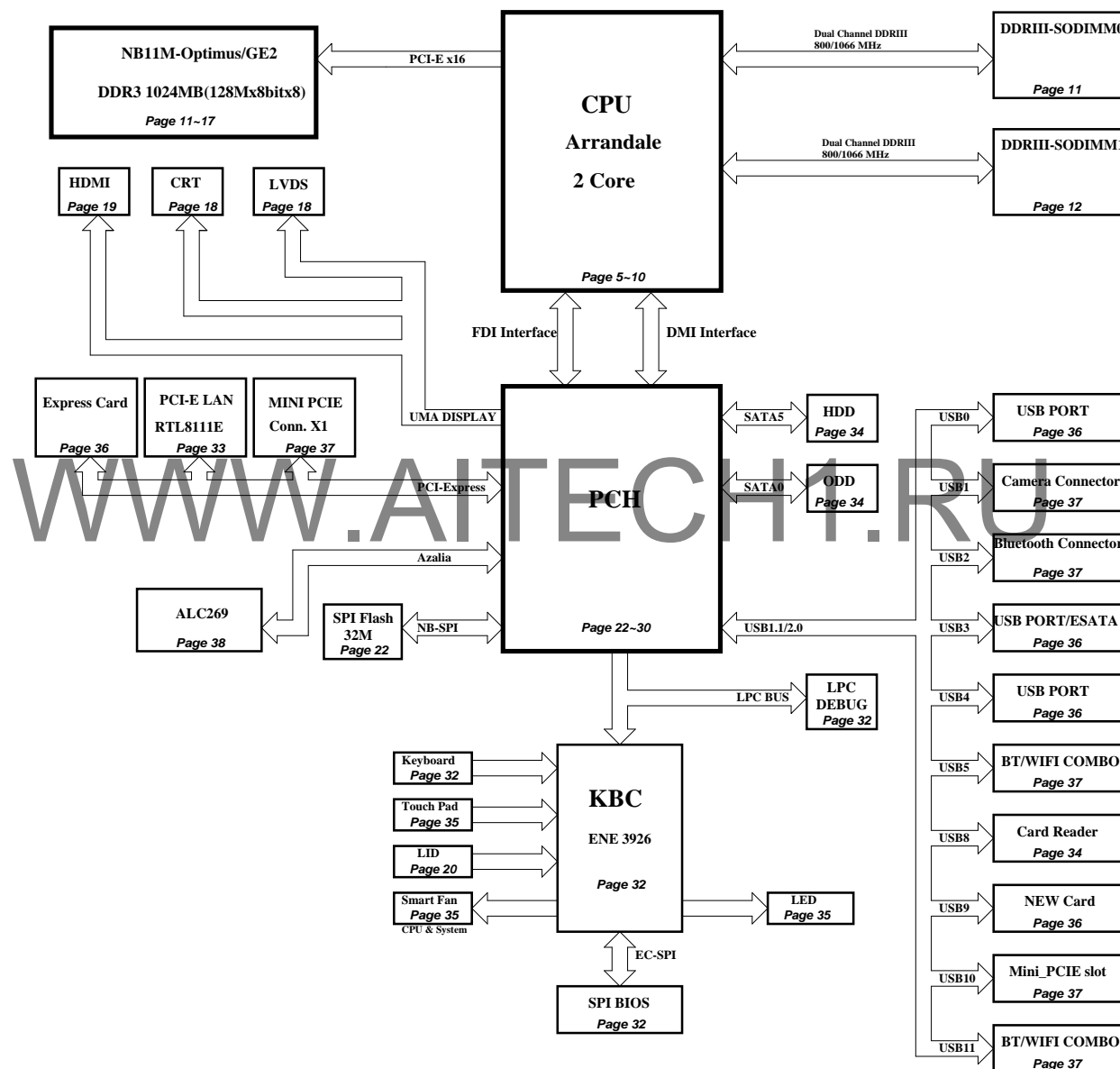
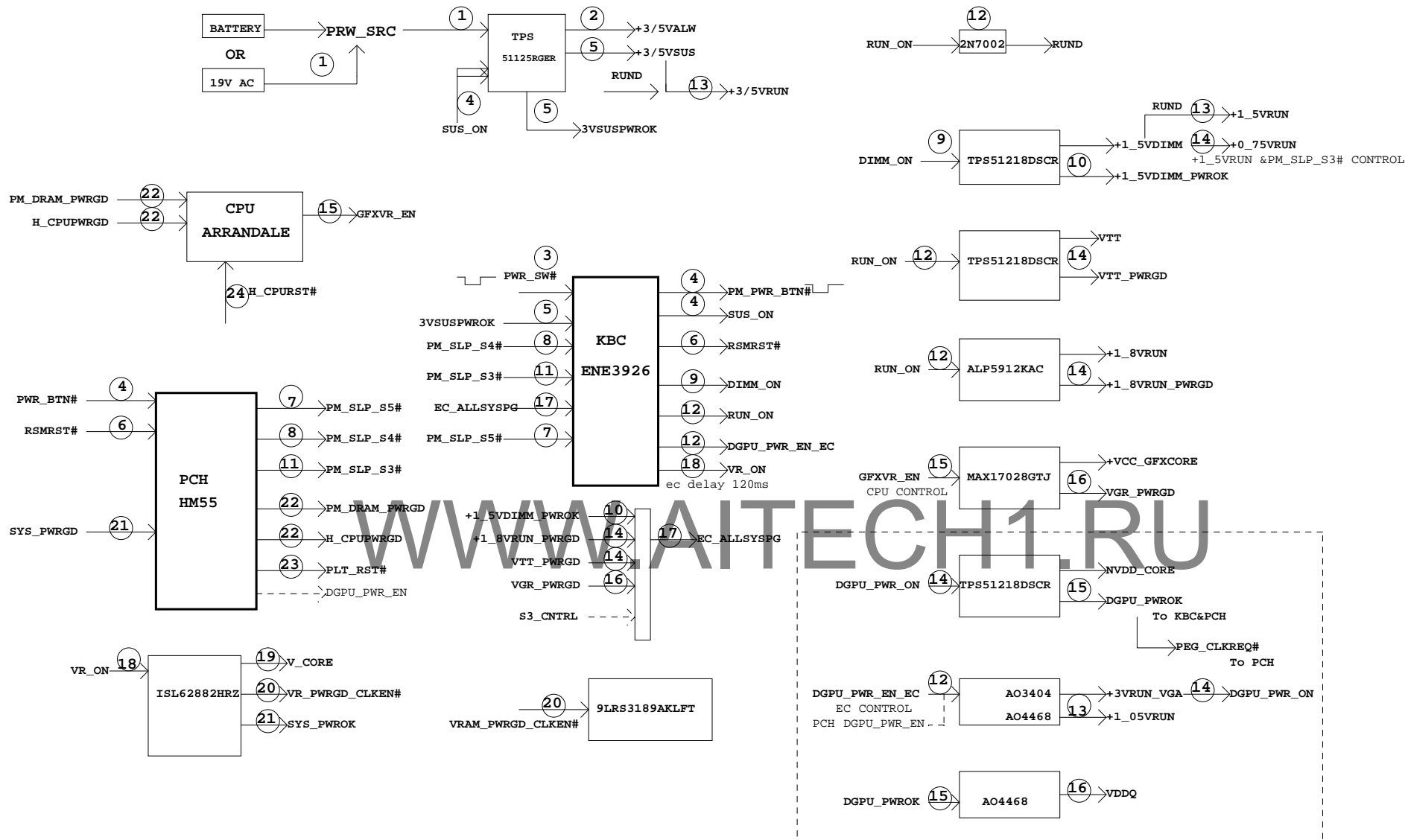


Table of Contents

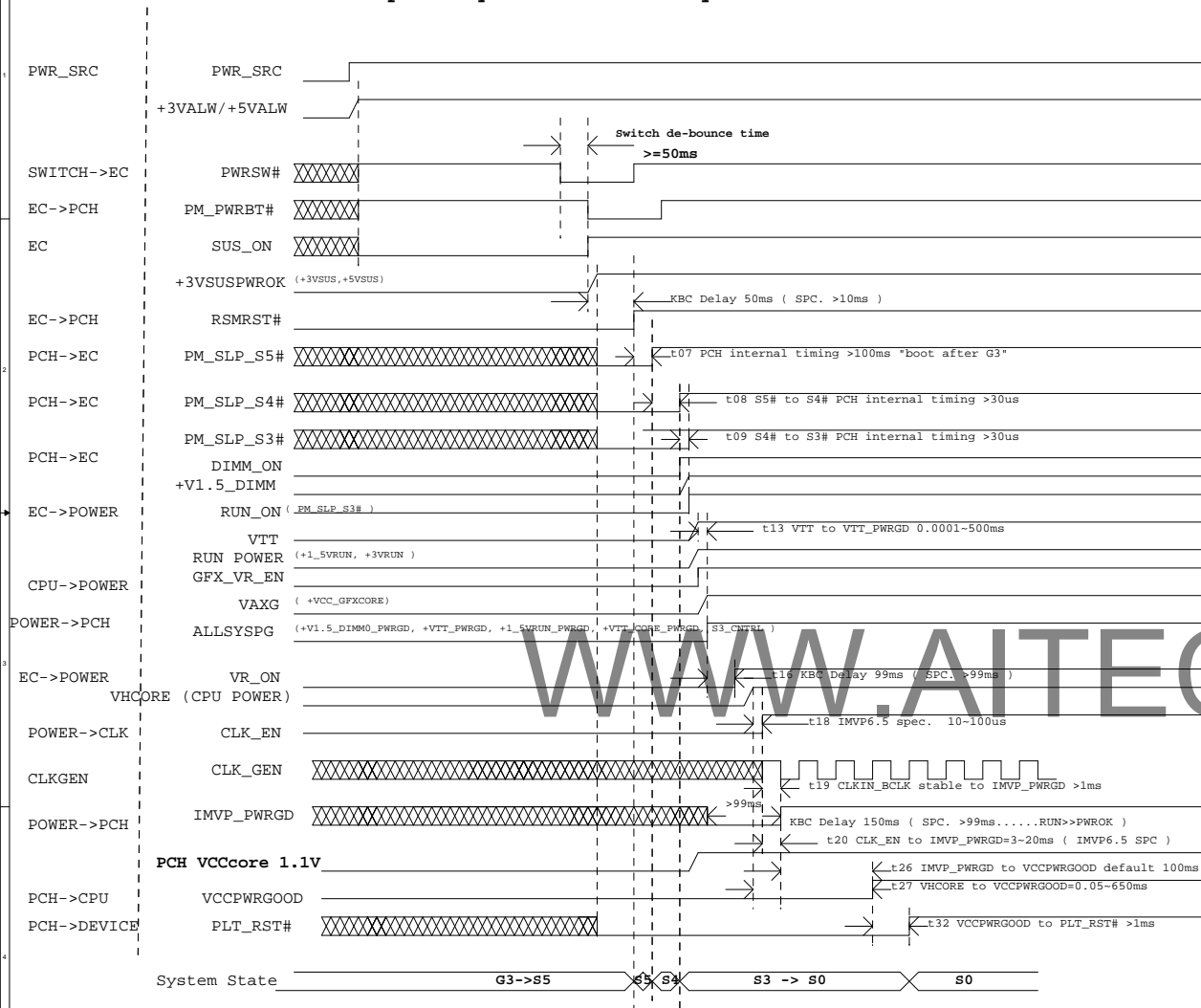
Page Description

01 : BLOCK DIAGRAM
02 : Power Delivery
03 : Power Sequency
04 : Clock/SMBus Distribution
05 : PROCESSOR-1 (HOST BUS)
06 : PROCESSOR-2 (DDR3)
07 : PROCESSOR-3 (POWER)
08 : PROCESSOR-4 (GRAPHICS POWER)
09 : PROCESSOR-5 (GND)
10 : PROCESSOR-6 (RESERVE)
11 : DDR3 SODIMM 0
12 : DDR3 SODIMM 1
13 : NB11M_GE2(PCIE_Interface)
14 : NB11M_GE2(FB interface)
15 : NB11M_GE2(VRAMA)
16 : NB11M_GE2(VRAMB)
17 : NB11M_GE2(CRT/LVDS)
18 : NB11M_GE2(GPIO)
19 : NB11M_GE2(STRAPS)
20 : CRT,LVDS connector & LID
21 : LEVEL SHIFT&HDMI
22 : PCH-1 (HDA,JTAG,SATA)
23 : PCH-2 (PCI-E,SMBUS,CLK)
24 : PCH-3 (DMI,FDI,GPIO)
25 : PCH-4 (LVDS,DDI)
26 : PCH-5 (PCI,USB,NVRAM)
27 : PCH-6 (GPIO,VSS_NCTF,RSVD)
28 : PCH-7 (POWER)
29 : PCH-8 (POWER)
30 : PCH-9 (GND)
31 : Clock Generator (9LRS3199AKL)
32 : KBC/EC/uP (KB3926)
33 : PCI-E Lan (RTL8111E)
34 : Cardreader (UB6250)
35 : FAN,Lauch board
36 : HDD,CDROM,USB,NEWCARD,ESATA
37 : MINIPICIE,CAMERA,BLUETOOTH,SW
38 : CODEC(ALC269)
39 : M_Battery select
40 : M_Battery Charger
41 : M_System Power
42 : SMDDR_VTERM/1_5VRUN
43 : VTT POWER,+1.8VRUN
44 : M_CPU power
45 : M_Graphic Core
46 : NVVDD,+1.03VRUN
47 : Screw/ ME
48 : 168AA_USB BOARD
49 : 168AB_Lauch board
50 : EMI
51 : Change List

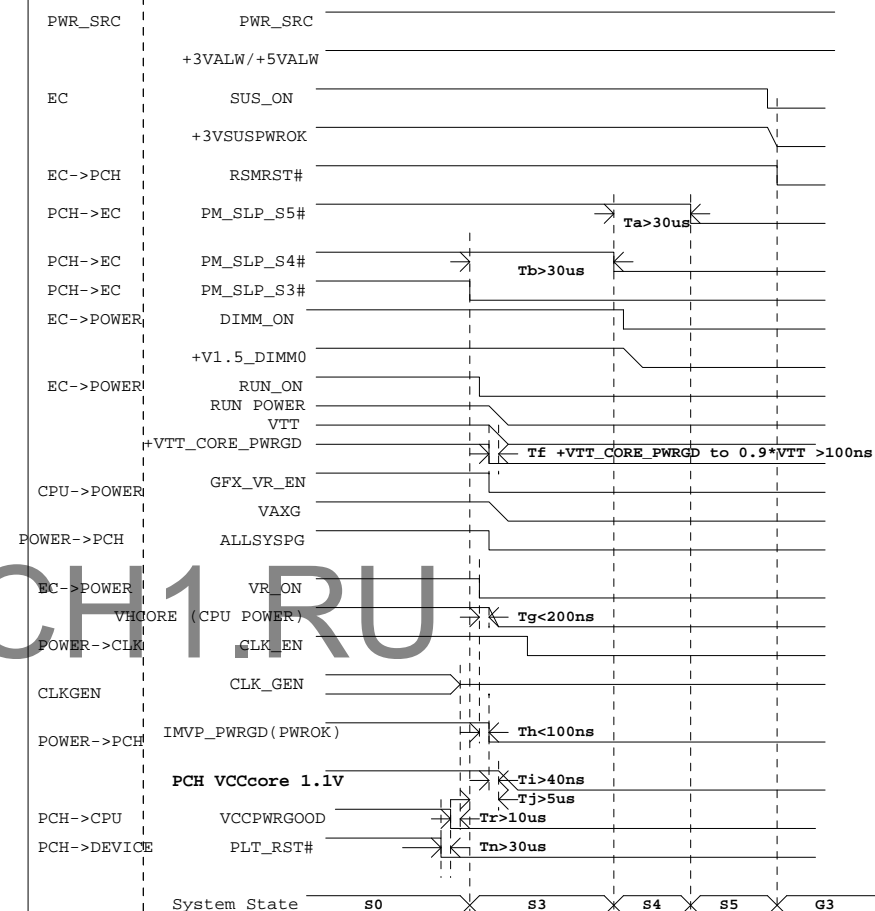


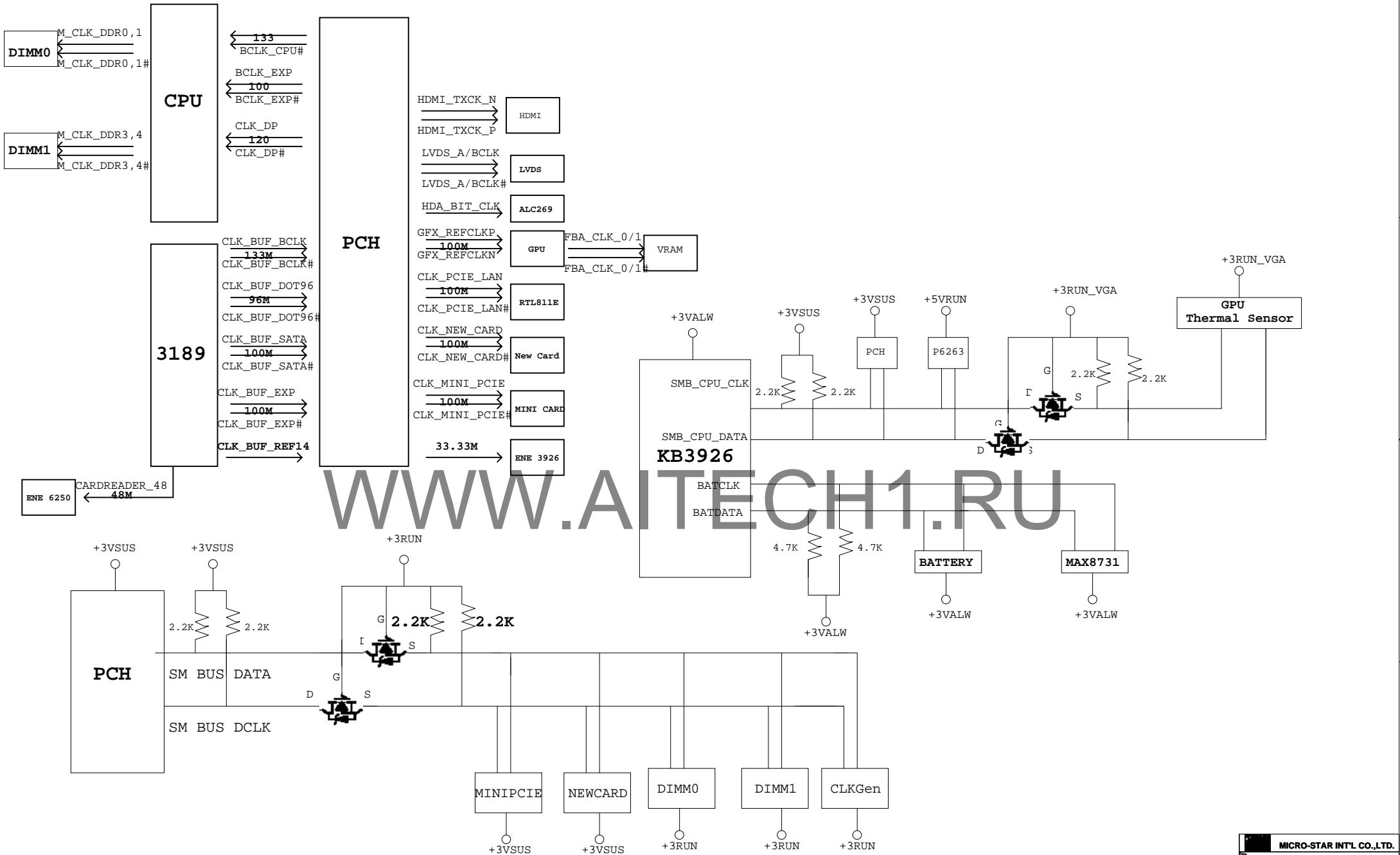


Calpella System Power on Sequence DC mode

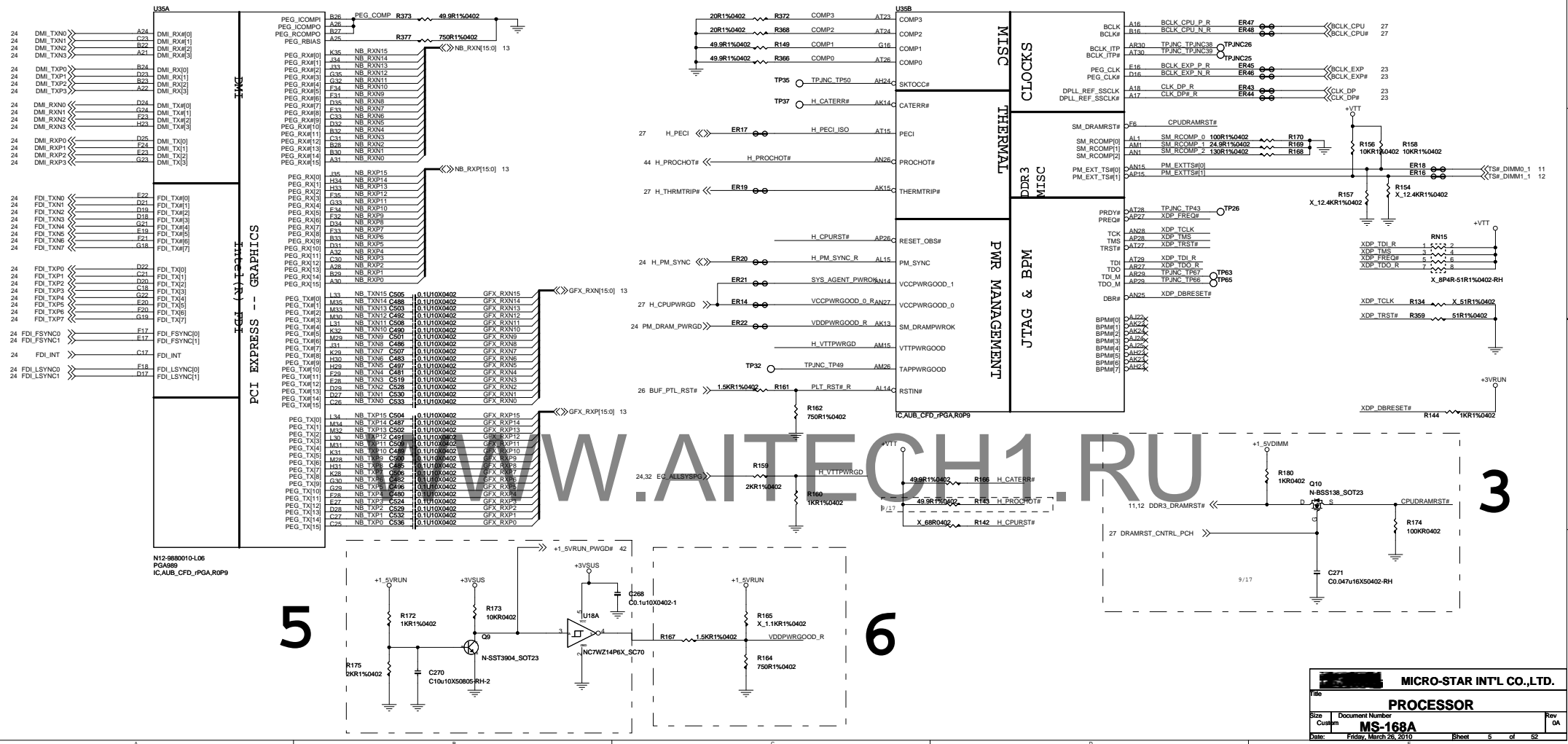


Power down Sequence DC mode S0 to G3

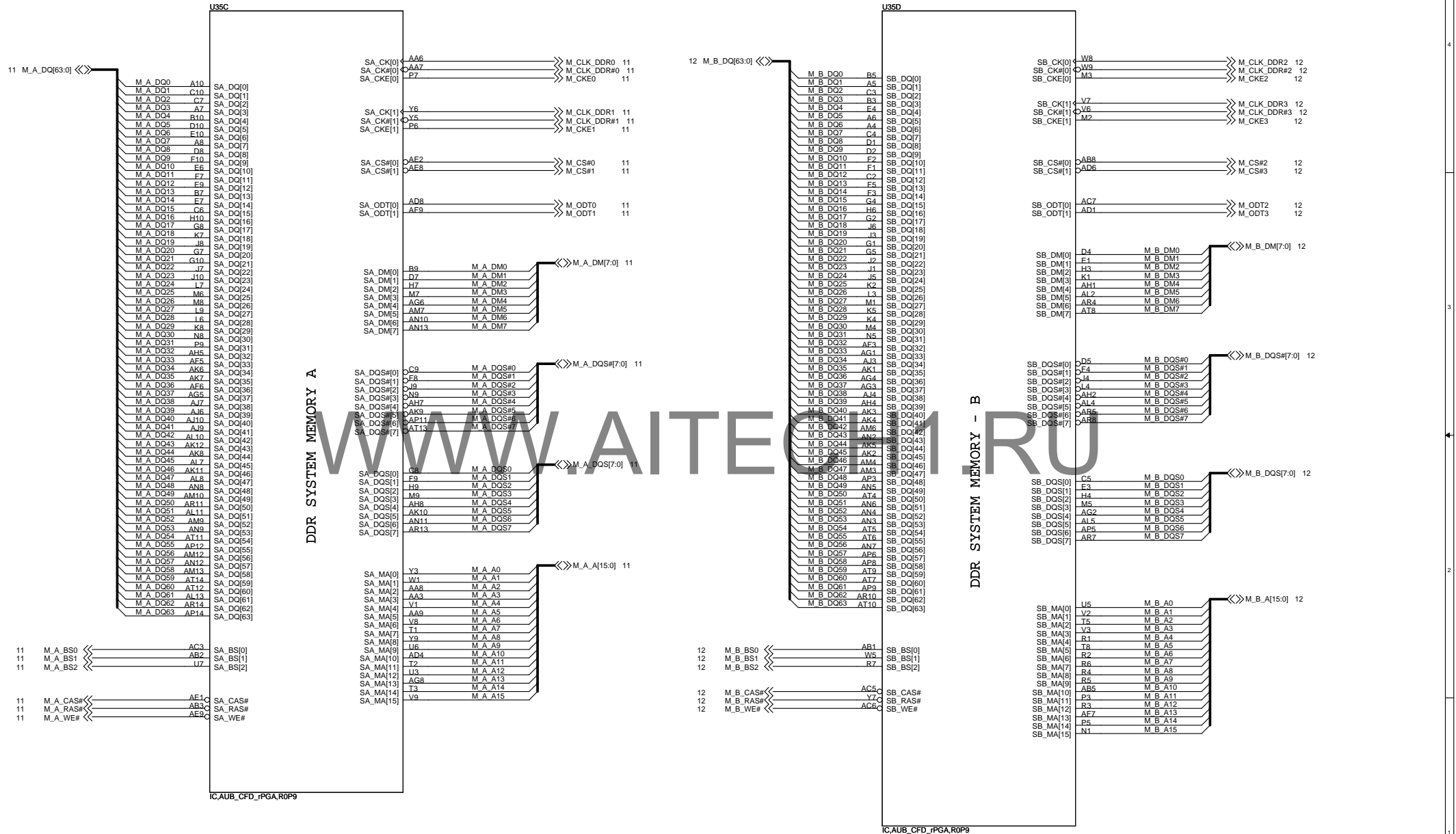




ARRANDALE PROCESSOR (CLK,MISC,JTAG)

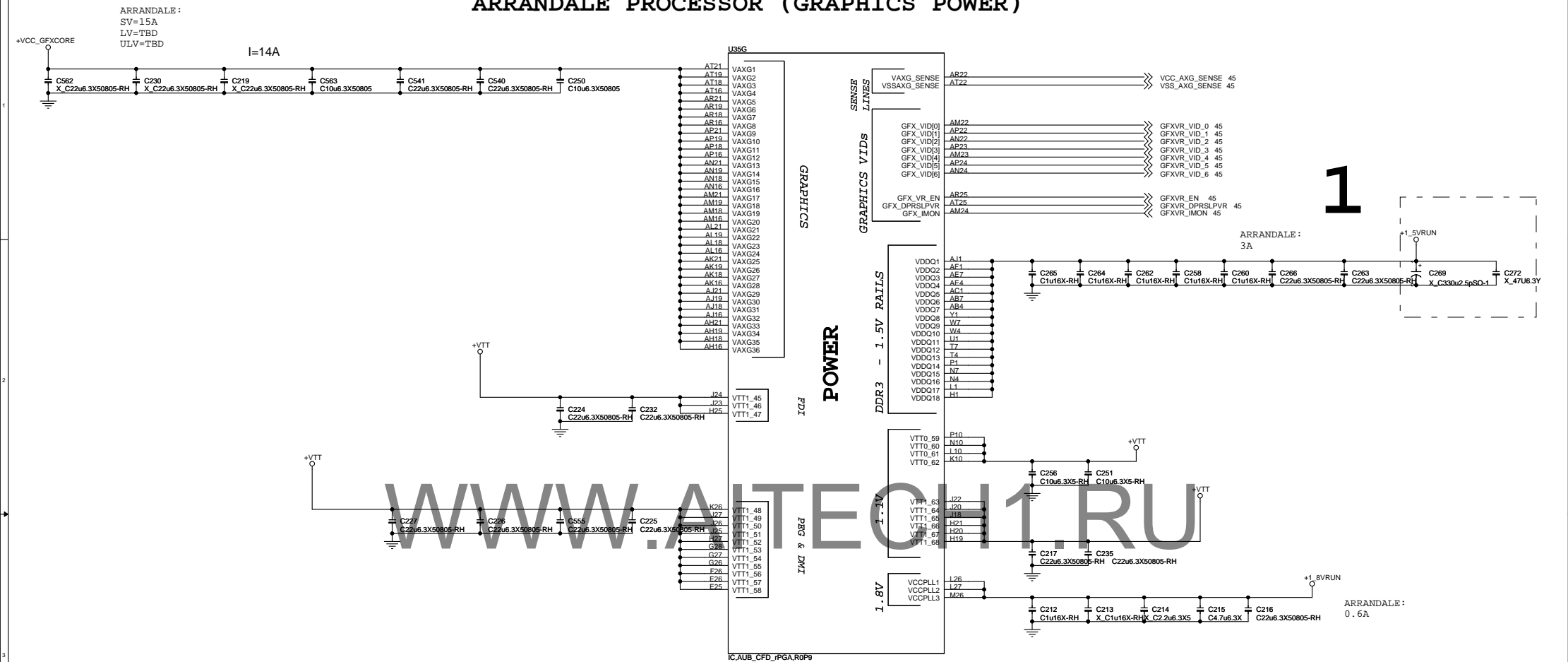


ARRANDALE PROCESSOR (DDR3)

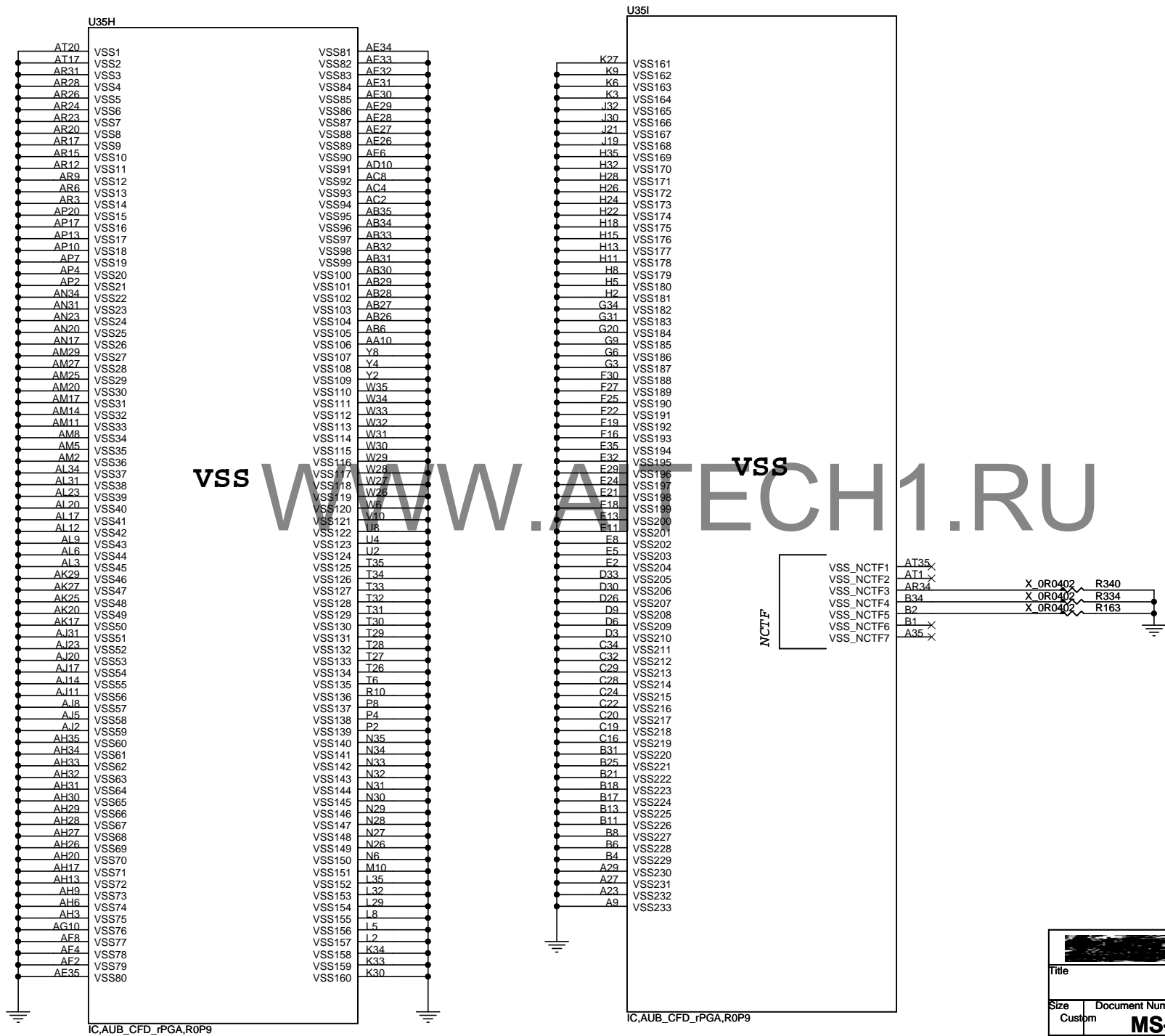



		MICRO-STAR INT'L CO.,LTD.	
Title			
PROCESSOR POWER			
Size	Document Number	Rev	
Custom	MS-168A	0A	
Date:	Friday, March 26, 2010	Sheet	7 of 52

ARRANDALE PROCESSOR (GRAPHICS POWER)

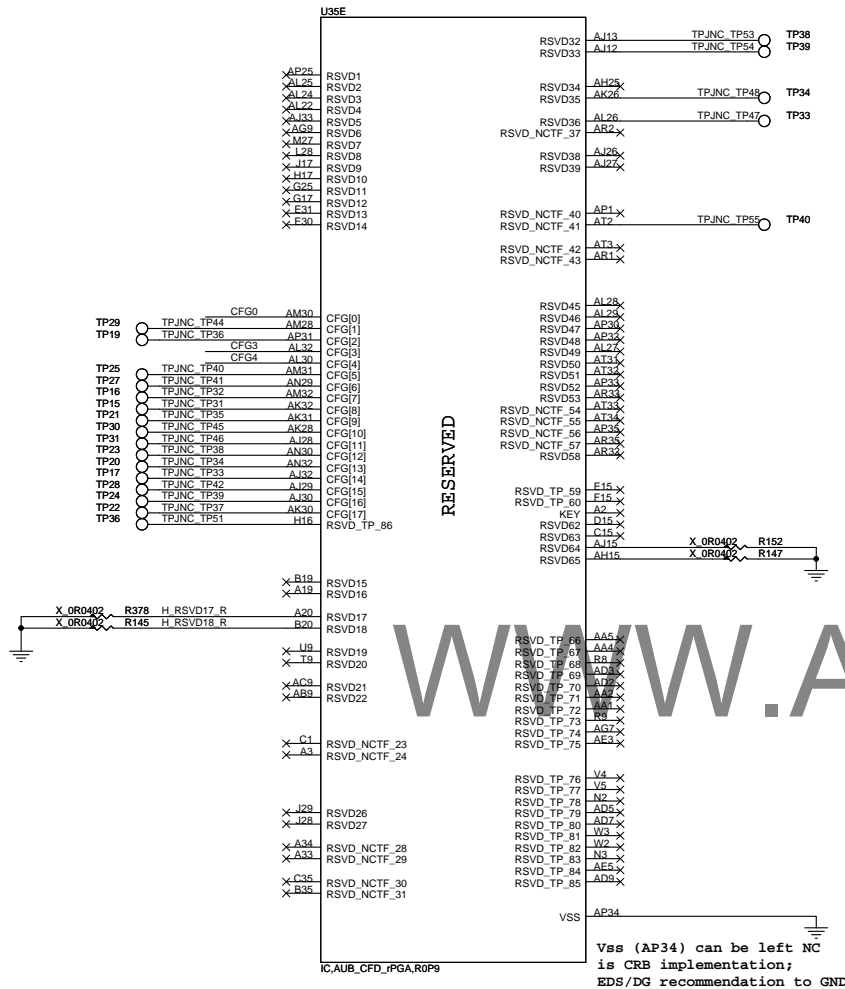


ARRANDALE PROCESSOR (GND)

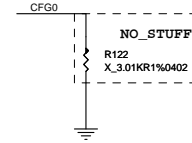


			MICRO-STAR INT'L CO.,LTD.		
Title					
PROCESSOR GND					
Size	Document Number				Rev
Custom	MS-168A				0A
Date:	Friday, March 26, 2010			Sheet	9 of 52

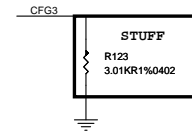
ARRANDALE PROCESSOR (RESERVED)



PCI-Express Configuration Select	
CFG0	1:Single FBS 0:Bifurcation enabled

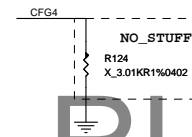


CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



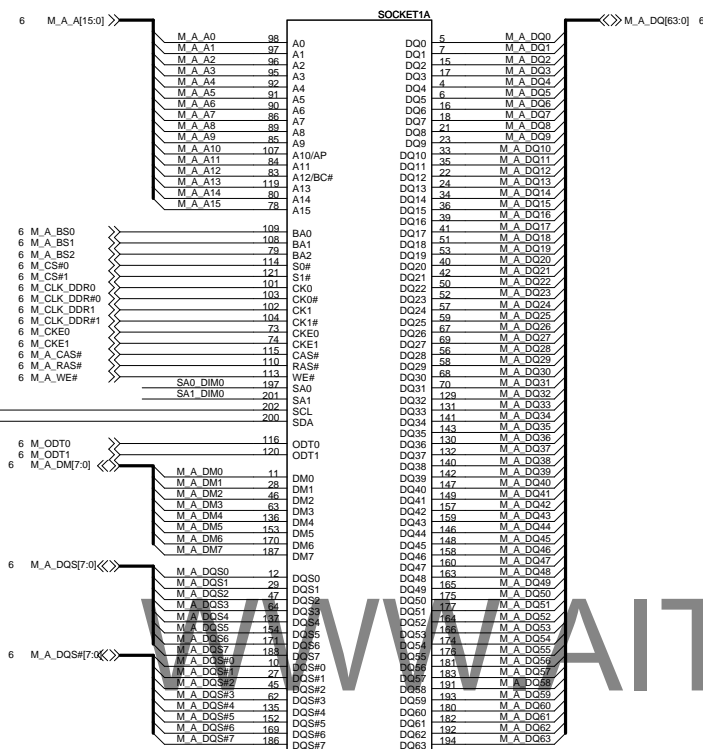
CFG3] PCI Express* Static Lane
Numbering Reversal. Lane Reversal will be
applied across all 16 Lanes.
1: No lane reversal
0: Reversal

CFG4 - Display Port Presence	
CFG4	1:Disabled: No Physical Display Port attached to Embedded Display Port 0:Enabled: An external Display Port device is connected to the Embedded Display Port

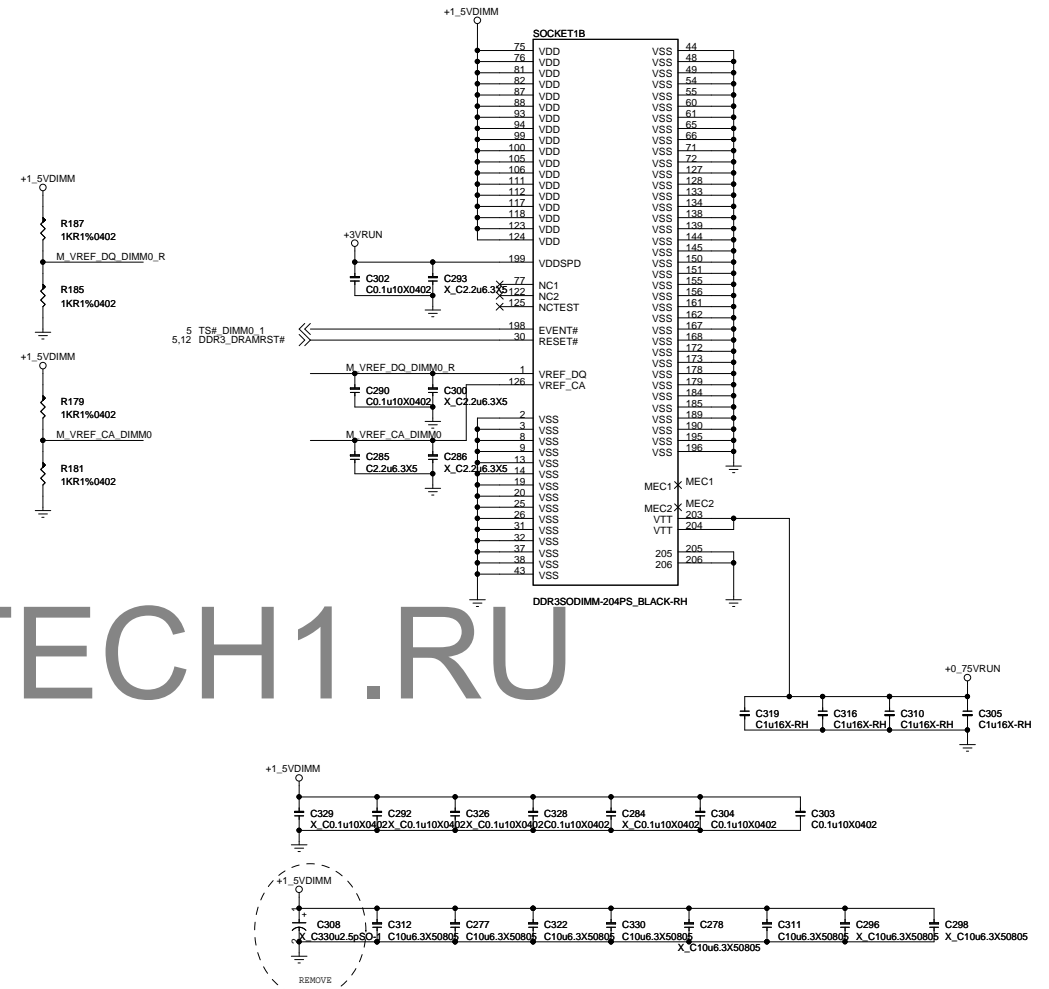


Layout Note:
Location of all CFG strap resistors needs
to be close to trace to minimize stub

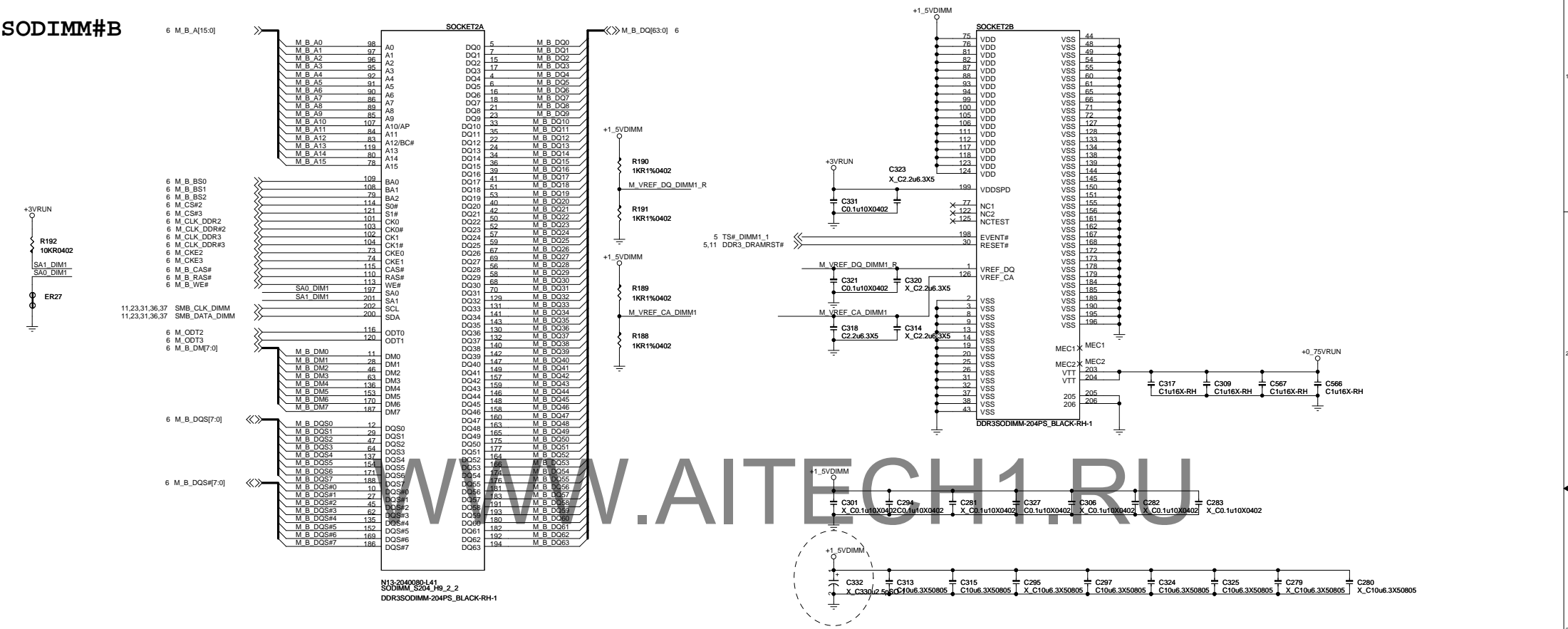
WWW.AITECH1.RU

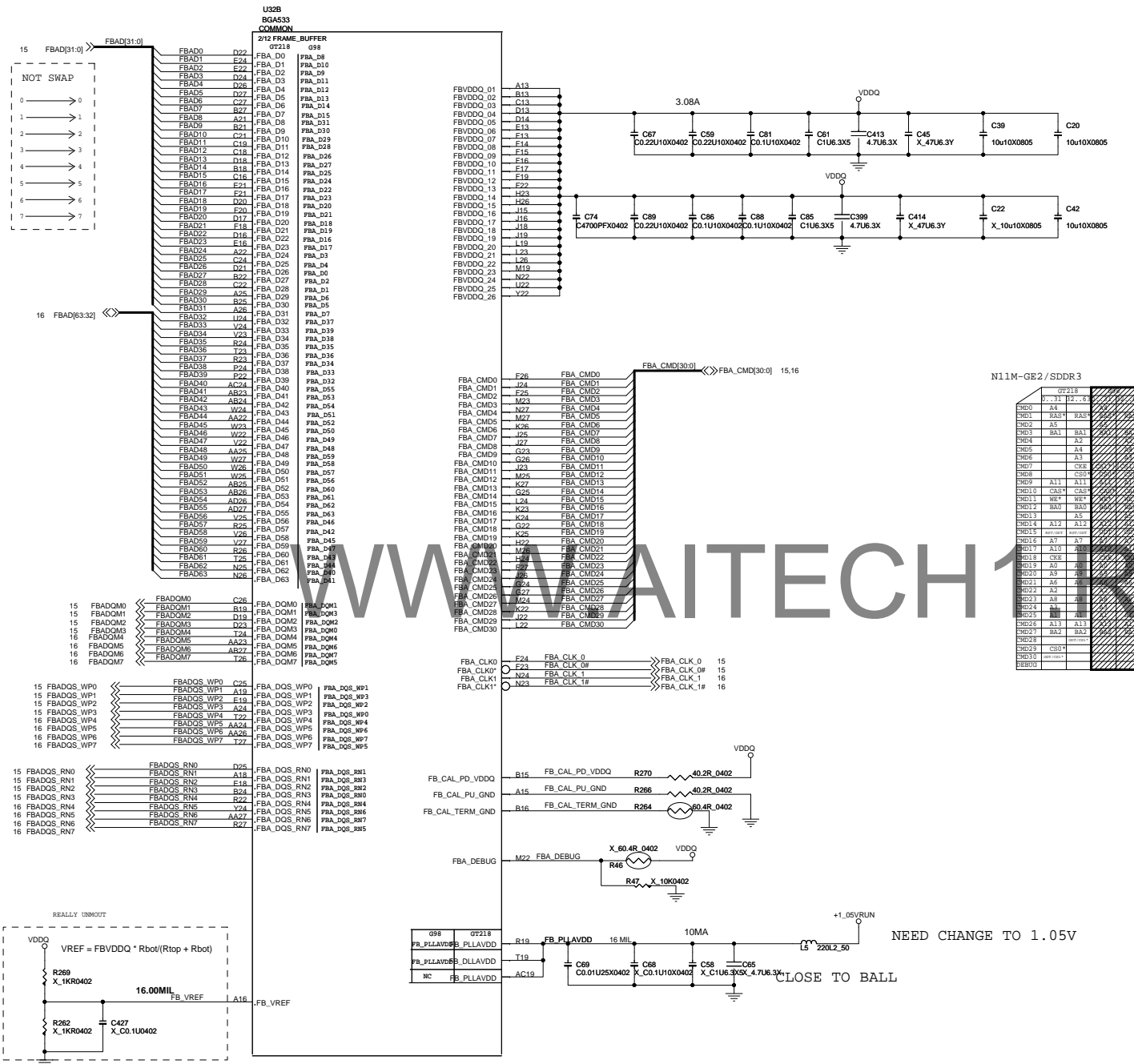
SODIMM#A

N13-2040060-L41
SODIMM_S204_H5_2
DDR3SODIMM-204PS_BLACK-RH

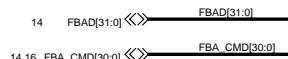


SODIMM#B

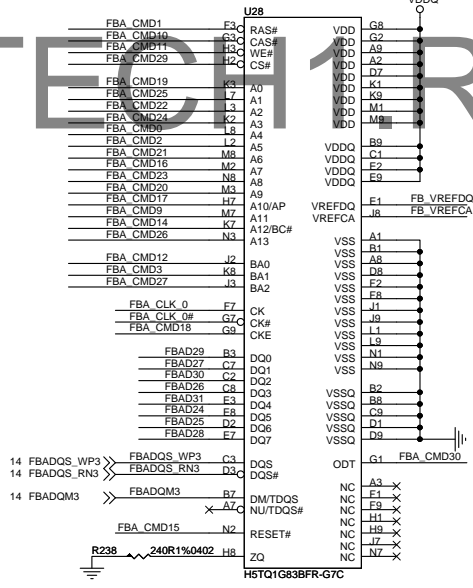
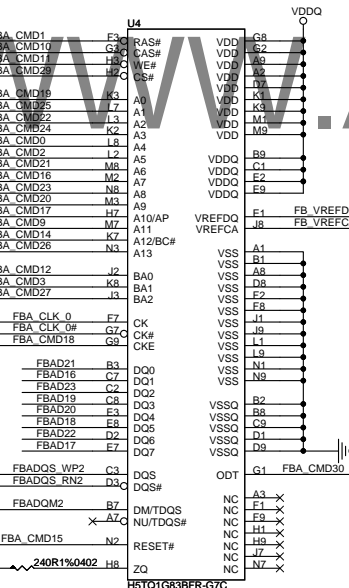
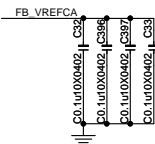
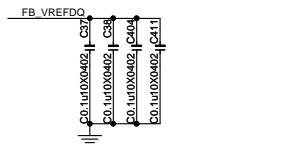
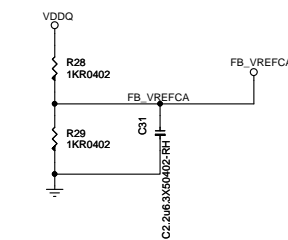
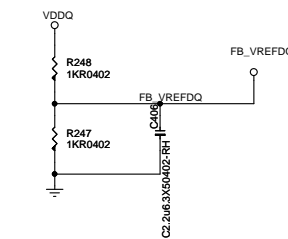
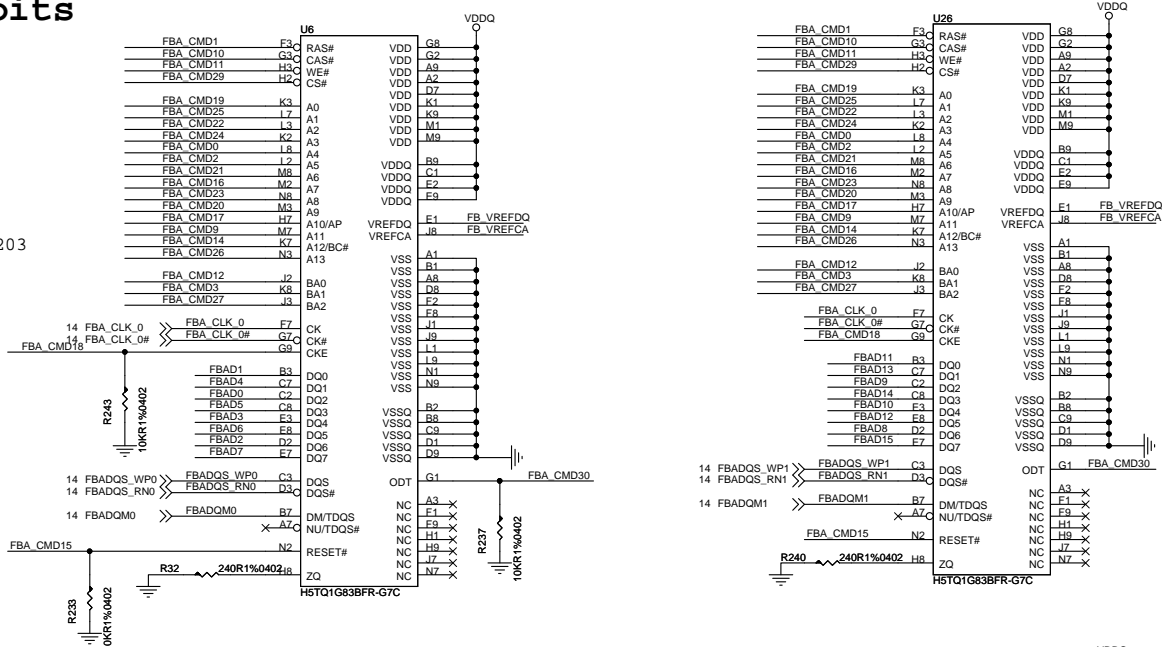




DDR3 128Mx8bits



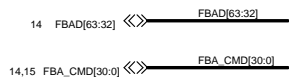
R252 need change to 242 ohm.1203



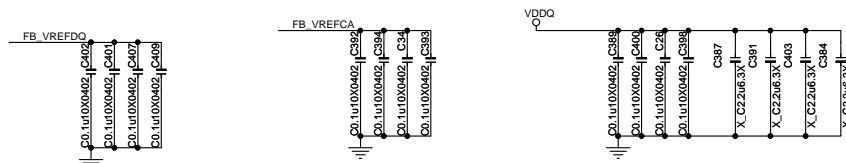
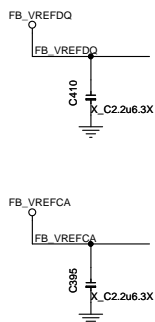
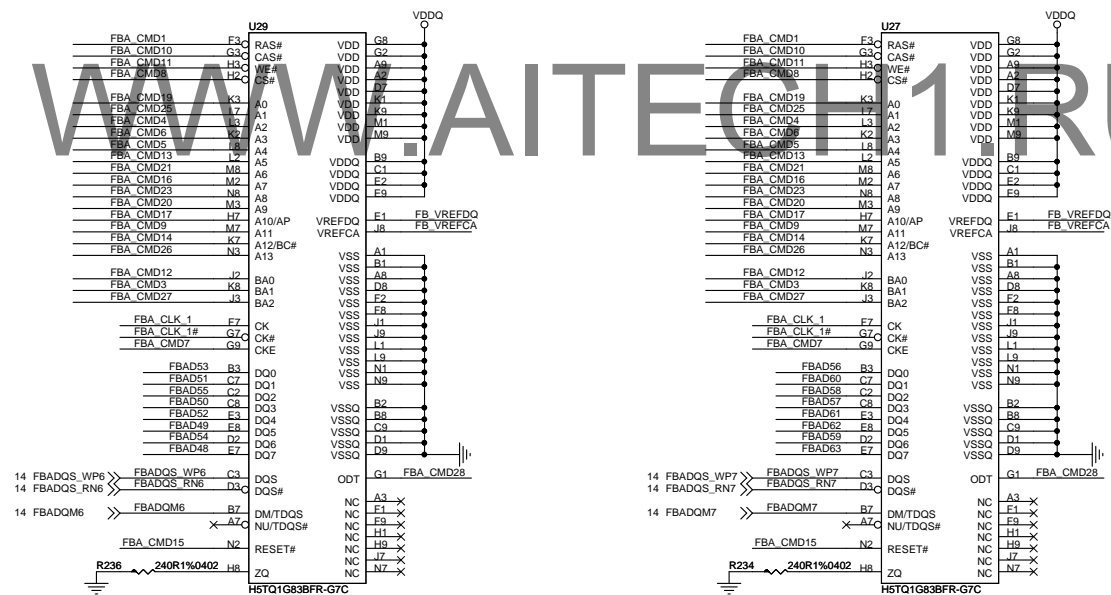
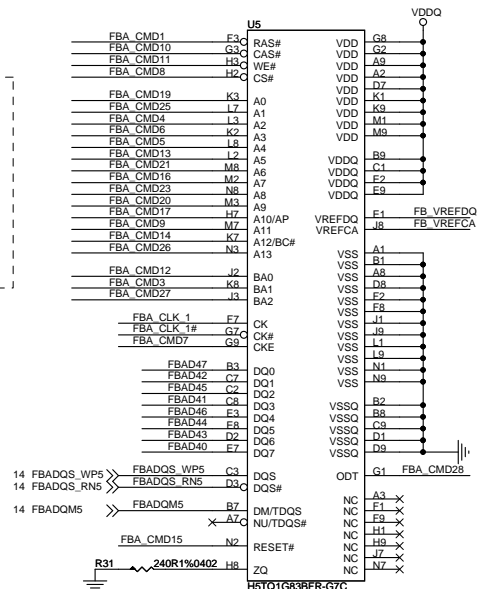
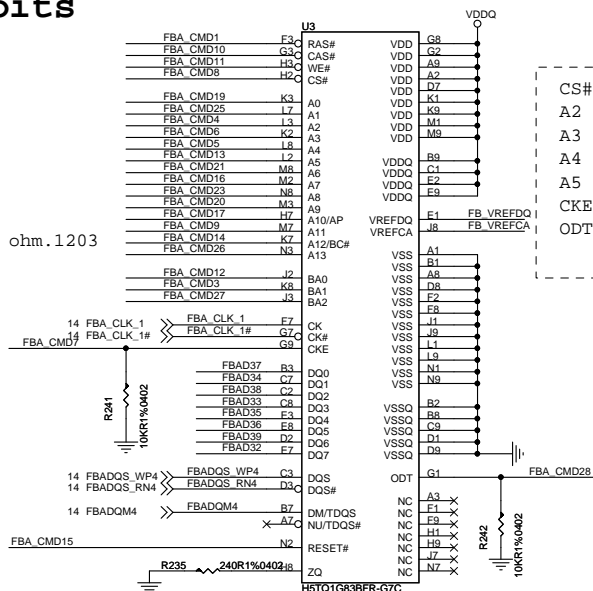
MSI CORPORATION		
Title		
PARK-POWER		
Size	Document Number	Rev
Custom	MS-168A	0A
Date:	Friday, March 26, 2010	Sheet 15 of 52

Each group(top & bottom) put a 0.1uF

DDR3 128Mx8bits

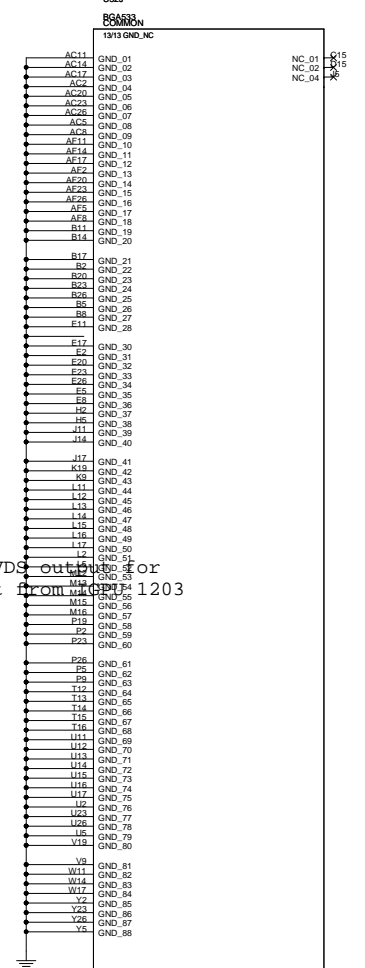
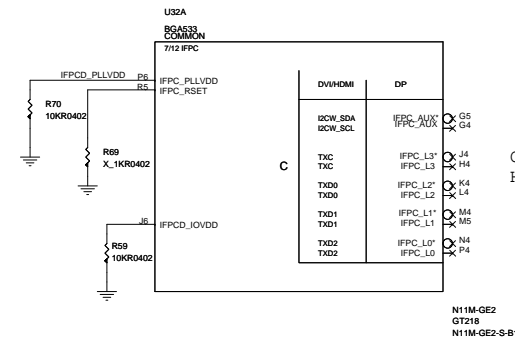
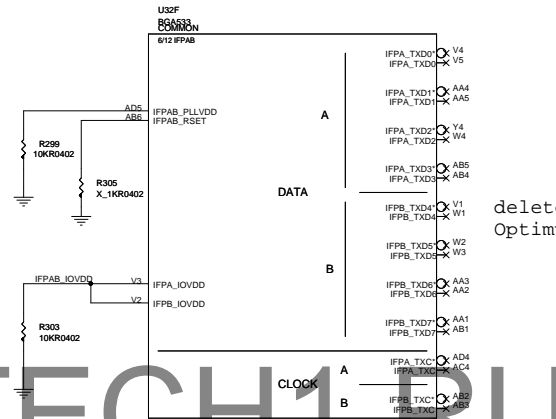
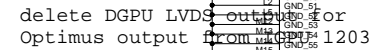


R264 need change to 242 ohm.1203

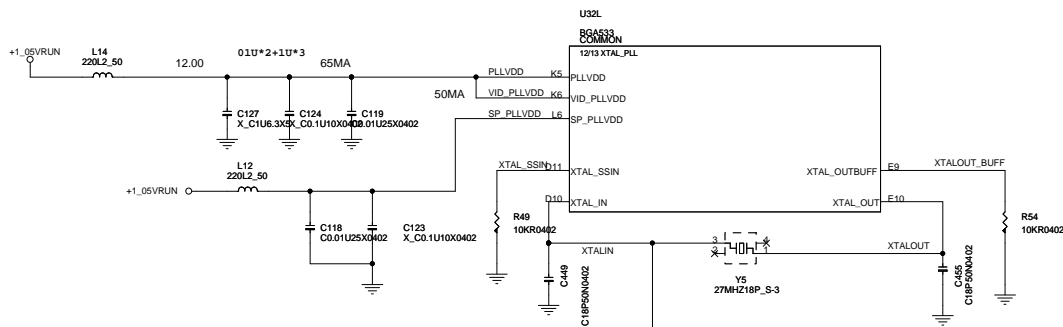


Each group(top & bottom) put a 0.1uF

MSI CORPORATION			
Title PARK-power straps			
Size Custom	Document Number MS-168A		Rev 0
Date:	Friday, March 26, 2010	Sheet	16 of 52



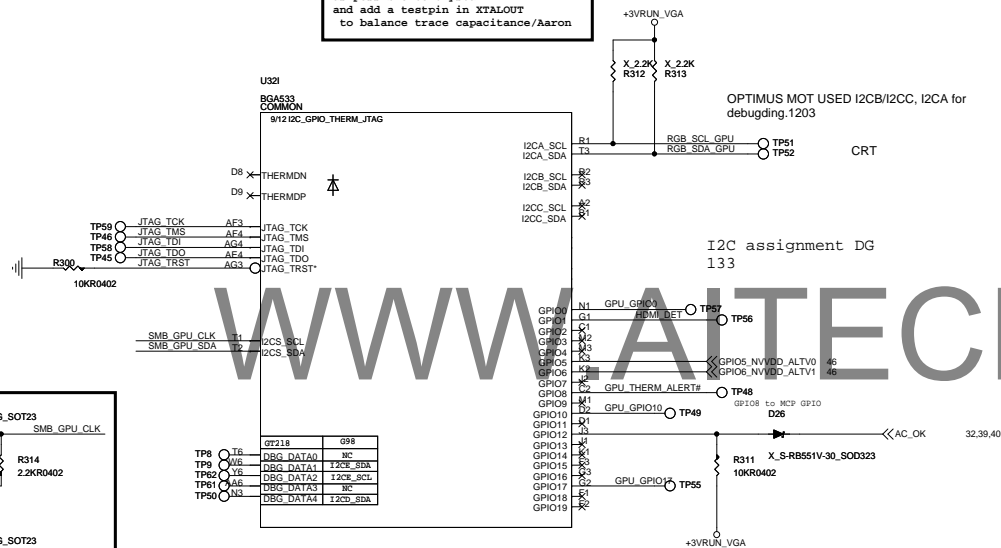
```
OPTIMUS not use GPU
HDMI, delete 1203
```



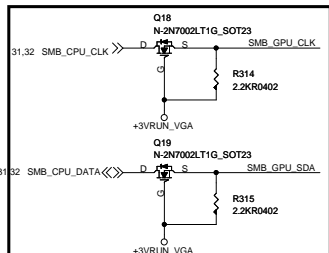
31 27M_OSC

X_0R0402 R297

Place this resistor as close as possible to crystal and add a testpin in XTALOUT to balance trace capacitance/Aaron



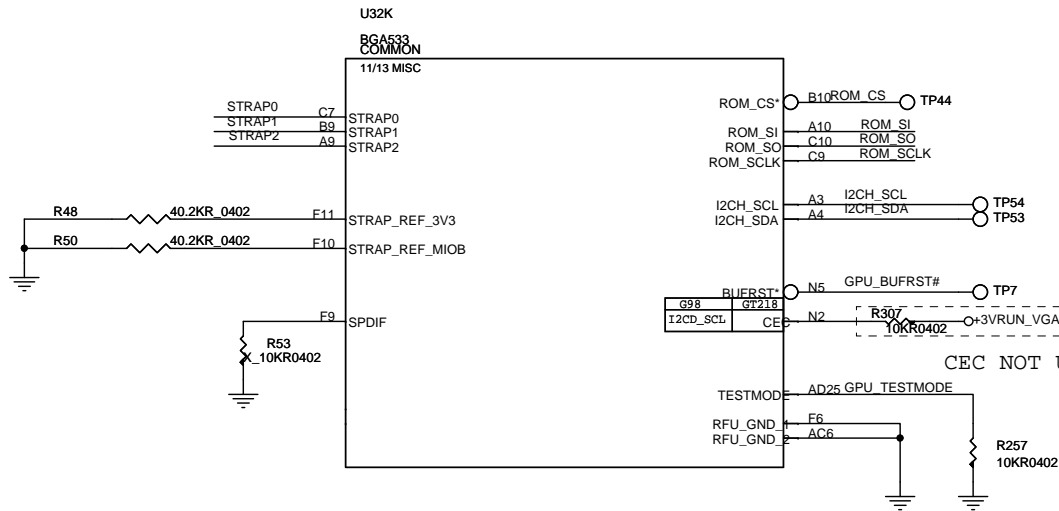
When use GPIO. Need Pull high or pull LOW.



For Optimus system VGA no power @IGP mode I203/zong

GPIO USAGE			
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	HDMI HOTPLUG DETECT
1	IN	N/A	DVI/HDMI LINKC HOTPLUG DETECT
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVDD ALT0
6	OUT	HIGH	NVDD ALT1
7	OUT	HIGH	FBVDD VDD0
8	IN	LOW	OVERTEMP ALERT
9	OUT	LOW	THERMAL ALERT
10	OUT	HIGH	DYNAMIC FB VREF GDDR3 (not used for DDR2)
11	OUT	HIGH	SLI SYNC0 (not used for GB1-64)
12	IN	N/A	AC DETECT
13	OUT	LOW	POWER SUPPLY CONTROL0
14	OUT	HIGH	POWER SUPPLY CONTROL1
15	IN	N/A	HPD_E
16	IN	N/A	DVI_E
17	IN	N/A	HDMI_E
18	IN	N/A	DVI_F (not used)
19	IN	N/A	HDMI_F (not used)

GPIO6	GPIO5	NVDD(N10M-SE1)
1	1	1.03V
1	0	0.85
0	1	TDB
0	0	0.85



CEC NOT USED 1130

N10M SE1

STRAP0	USER 3	1
PU 45K	USER 2	1
	USER 1	1
	USER 0	1
STRAP1	3GIO_PADCFG 3	0
PU 35K	3GIO_PADCFG 2	0
	3GIO_PADCFG 1	0
	3GIO_PADCFG 0	1
STRAP2	PCI_DEVID3	0
PD 5K	PCI_DEVID2	0
	PCI_DEVID1	0
	PCI_DEVID0	0
ROM_SCLK	PCI DEVID 4	1
PU 15K	SUBVENDOR	0
	SLOT_CLK	1
	PEX_PLL_EN	0
ROM_SI	RAMCFG 3	0
PD 5K	RAMCFG 2	0
	RAMCFG 1	0
	RAMCFG 0	0
ROM_SO	XCLK_417	1
PD 10K	FB_0_BAR_SIZE	0
	SMB_ALT_ADDR	0
	VGA_DEVICE	0

SM BUS define resolution 1111

PUN-04992-001-V01
NOTEBOOK 0001

0X0A70 0000
NB11M-GE2

VBIOS is in system bios

GPU and MCH do not share a common clock


disable pci express PLL termination

SEE PUN update 1130

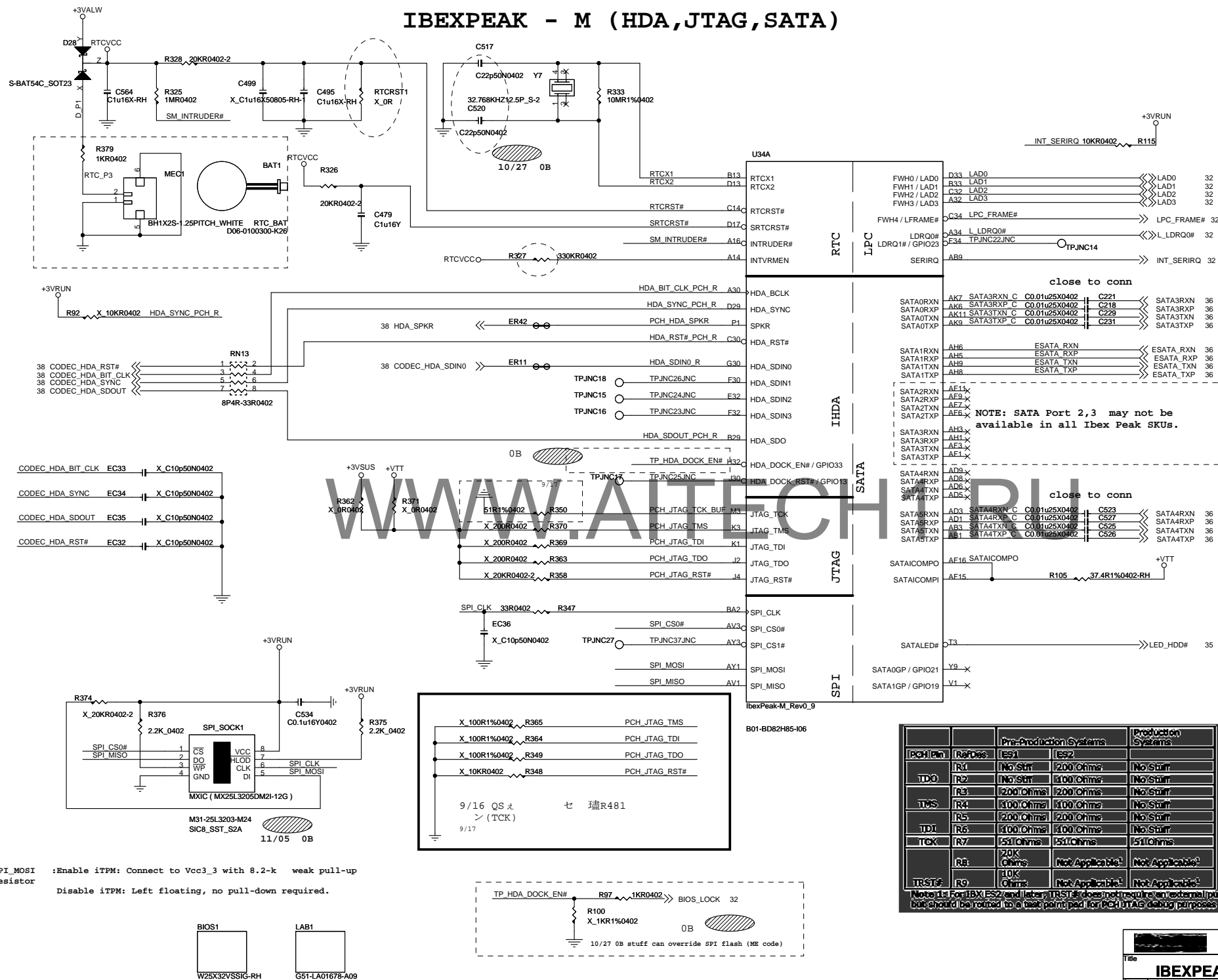
Have 27M hz CRYSTAL

SPEC have no TV function

Rvalue	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

 MICRO-STAR INT'L CO.,LTD.		
Title		
PARK MEM DDR3 A1		
Size	Document Number	Rev
B	MS-168A	0A
Date:	Friday, March 26, 2010	Sheet 19 of 52

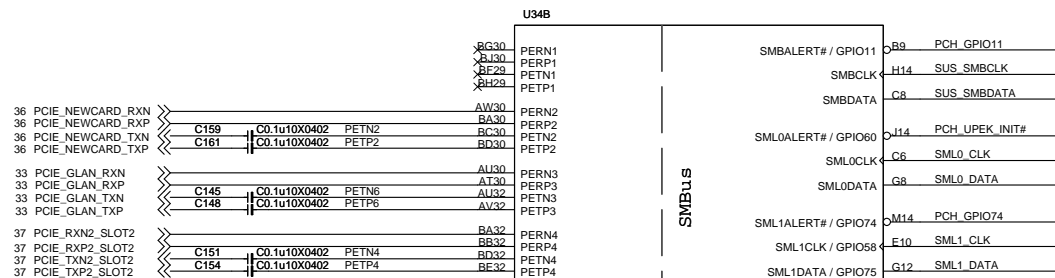
IBEXPEAK - M (HDA,JTAG,SATA)



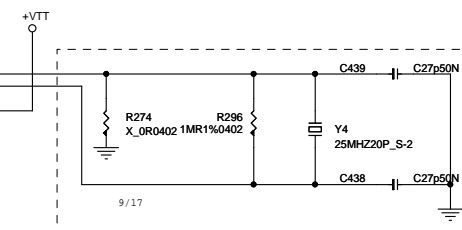
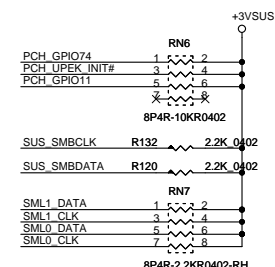
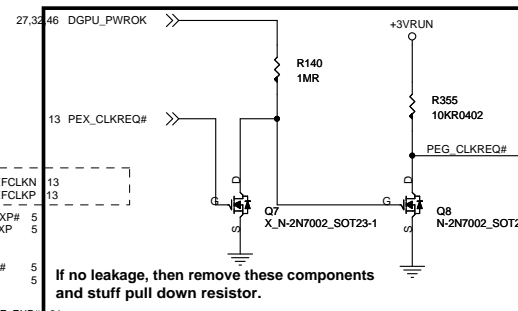
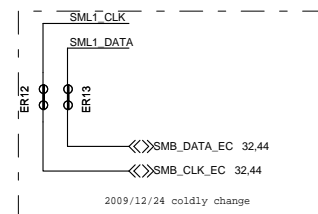
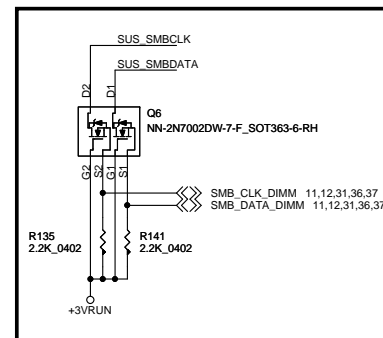
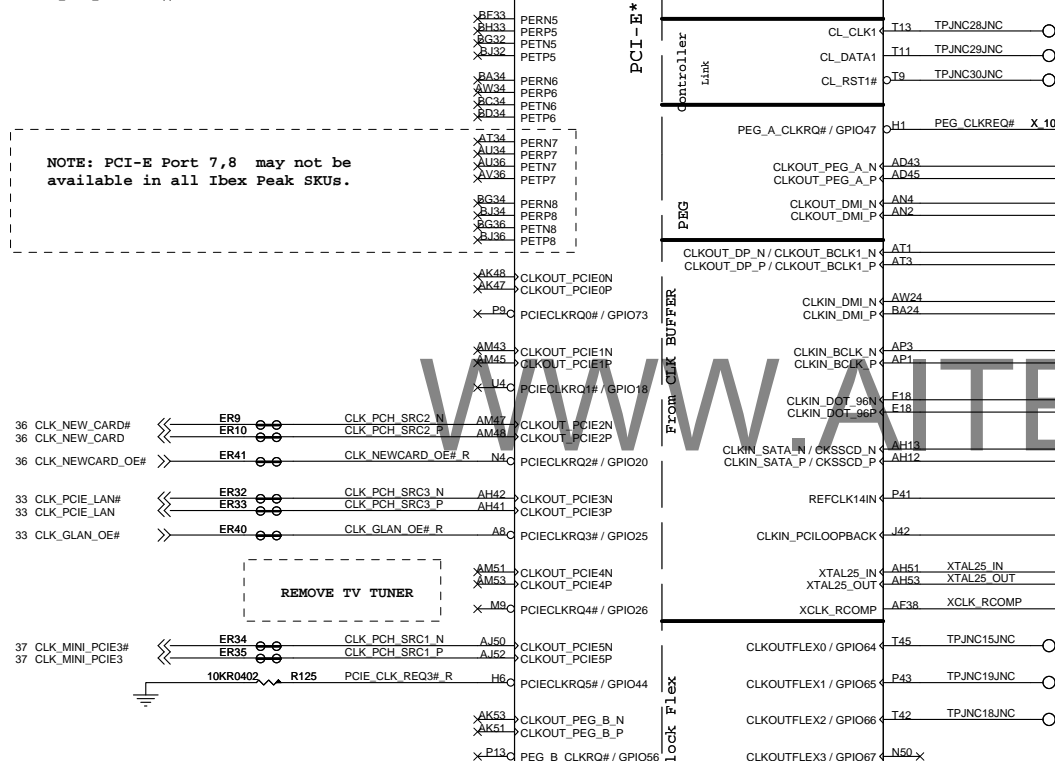
		Pre-Production Systems		Production Systems
PCH Pin	RefDes	ES1	ES2	
TD0	R1	No Stn	200 Ohms	No Stn
	R2	No Stn	100 Ohms	No Stn
	R3	200 Ohms	200 Ohms	No Stn
TMS	R4	100 Ohms	100 Ohms	No Stn
	R5	200 Ohms	200 Ohms	No Stn
TD1	R6	100 Ohms	100 Ohms	No Stn
TCK	R7	551 Ohms	551 Ohms	551 Ohms
	R8	20K Ohms	Not Applicable ¹	Not Applicable ²
TRST ³	R9	10K Ohms	Not Applicable ¹	Not Applicable ²

Notes: 1) For ES2 and later, TRST³ does not require an external pull-up, but should be routed to a test point pin for PCH UTAG debug purposes

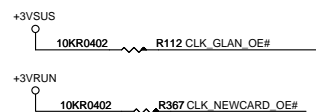
IBEXPEAK - M (PCI-E, SMBUS, CLK)



NOTE: PCI-E Port 7,8 may not be available in all Ibex Peak SKUs.



PCIECLKRQ1# / GPIO18 PCIECLKRQ1# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ#	SUS Well



IBEXPEAK - M (DMI,FDI,GPIO)

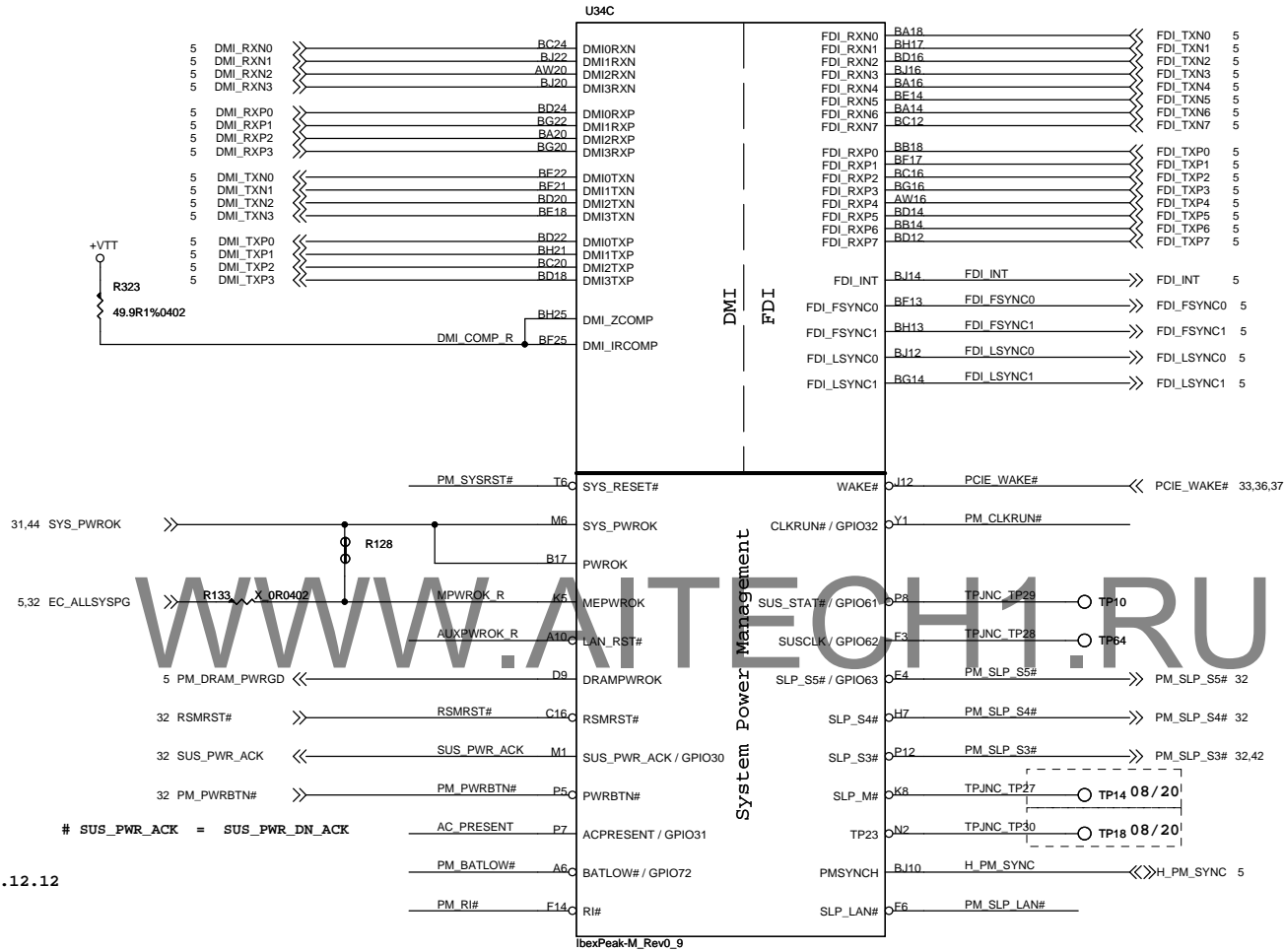
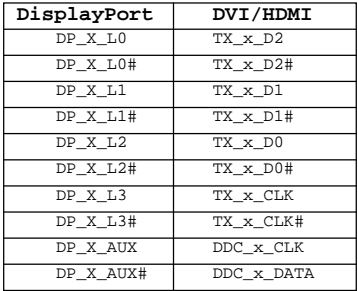


Diagram illustrating the connection of the DVI connector to the system components:

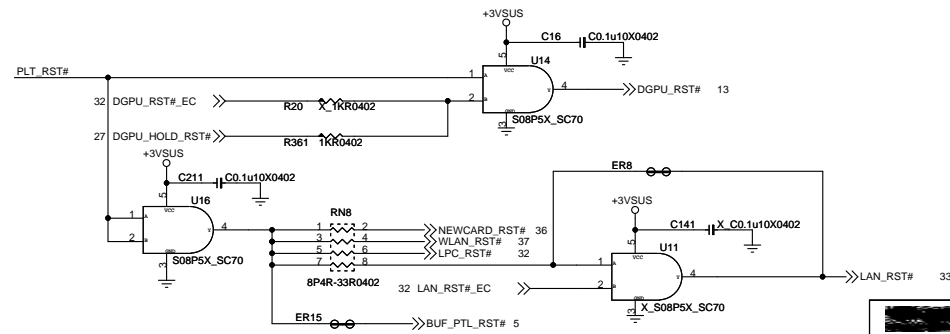
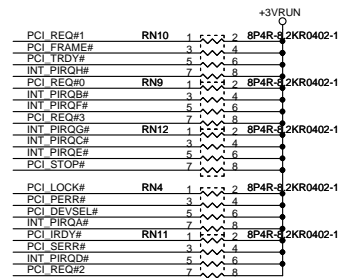
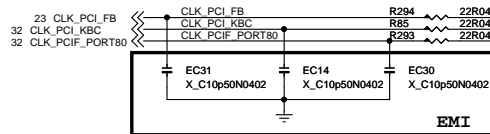
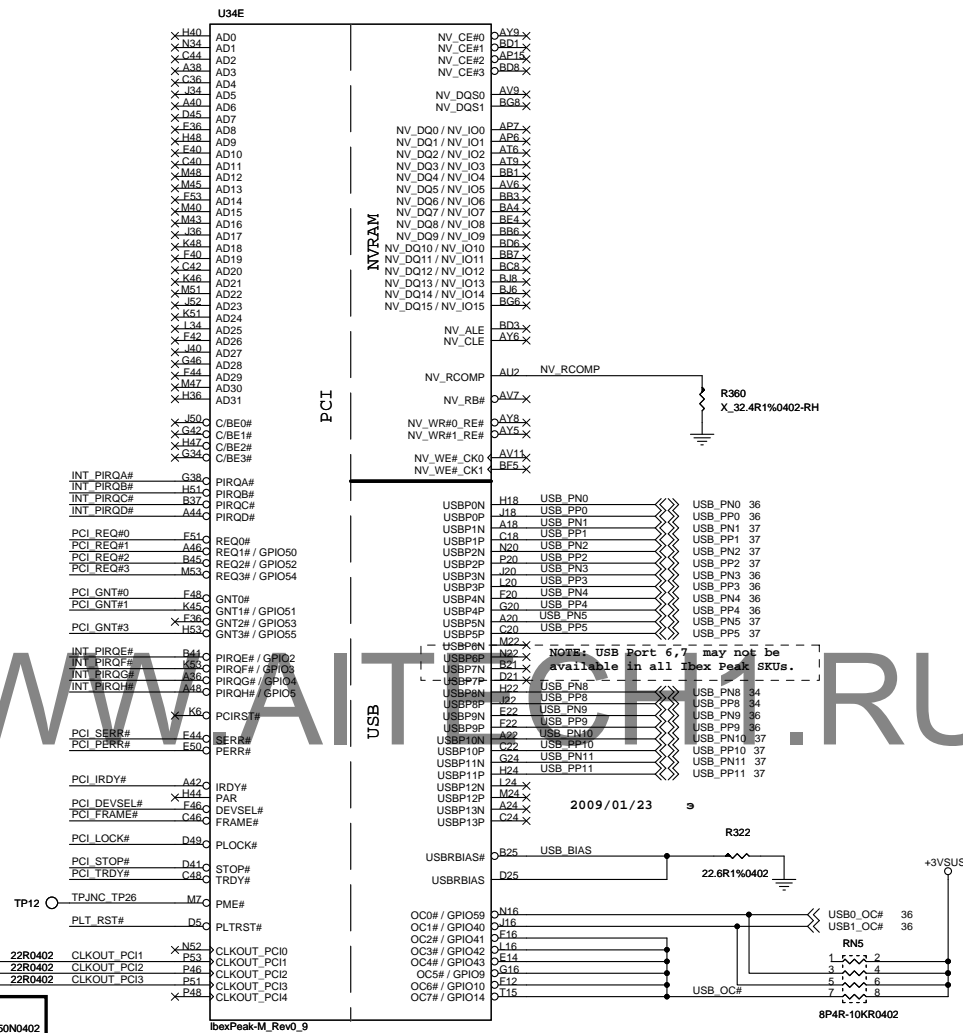
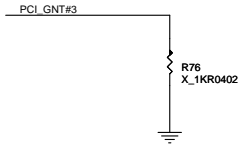
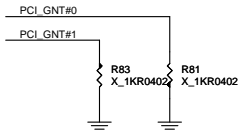
- System Components:**
 - AA52: CRT_BLUE
 - AB53: CRT_GREEN
 - AD53: CRT_RED
 - DDPC_CTRLCLK: DDPD_CTRLCLK
 - DDPC_CTRLDATA: DDPD_CTRLDATA
 - U50: DVI_CLK_UMA
 - U52: DVI_DATA_UMA
- Connections:**
 - AA52 is connected to CRT_BLUE.
 - AB53 is connected to CRT_GREEN.
 - AD53 is connected to CRT_RED.
 - DDPC_CTRLCLK is connected to DDPD_CTRLCLK.
 - DDPC_CTRLDATA is connected to DDPD_CTRLDATA.
 - U50 is connected to DVI_CLK_UMA.
 - U52 is connected to DVI_DATA_UMA.



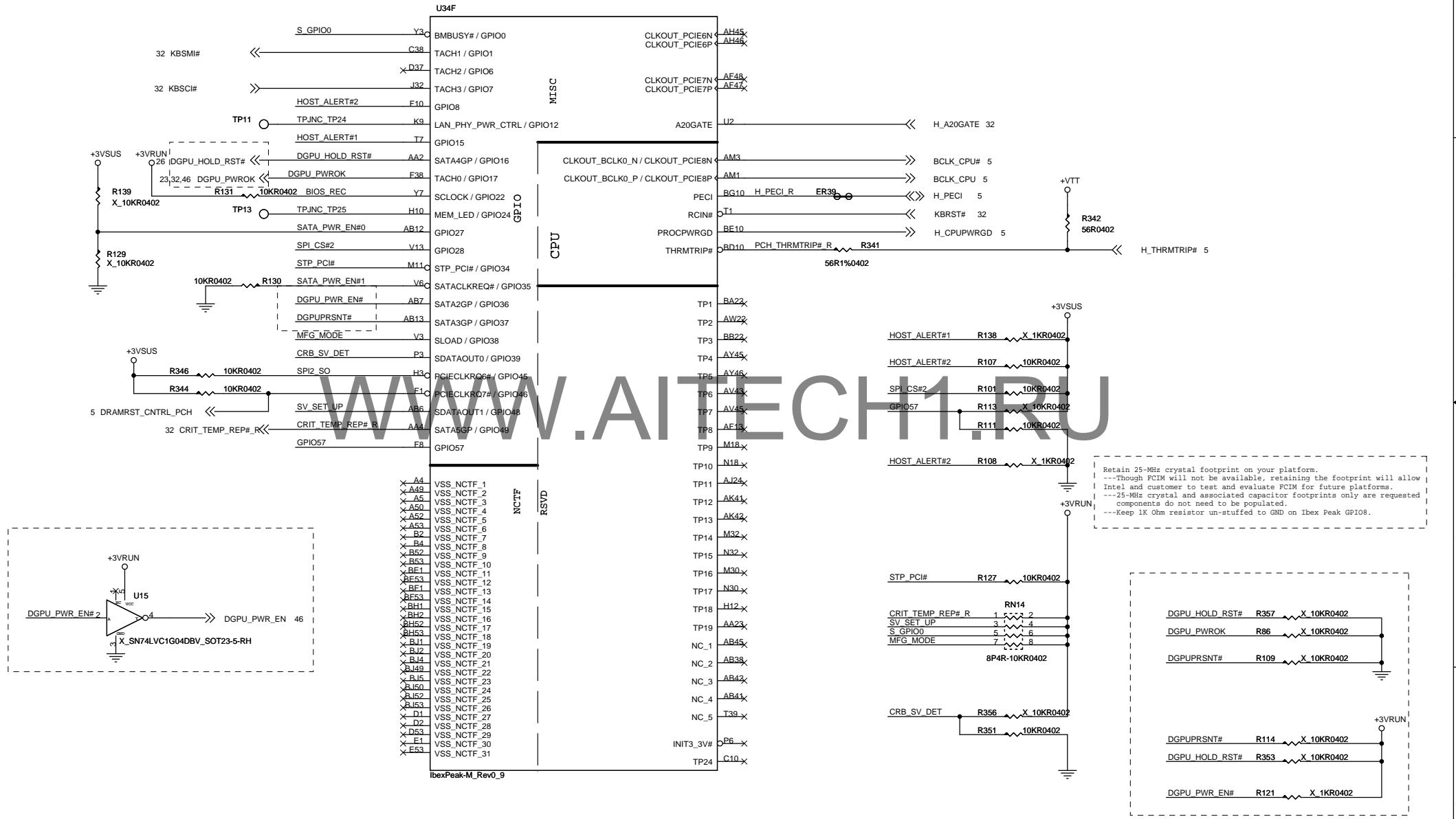
IBEXPEAK - M (PCI,USB,NVRAM)

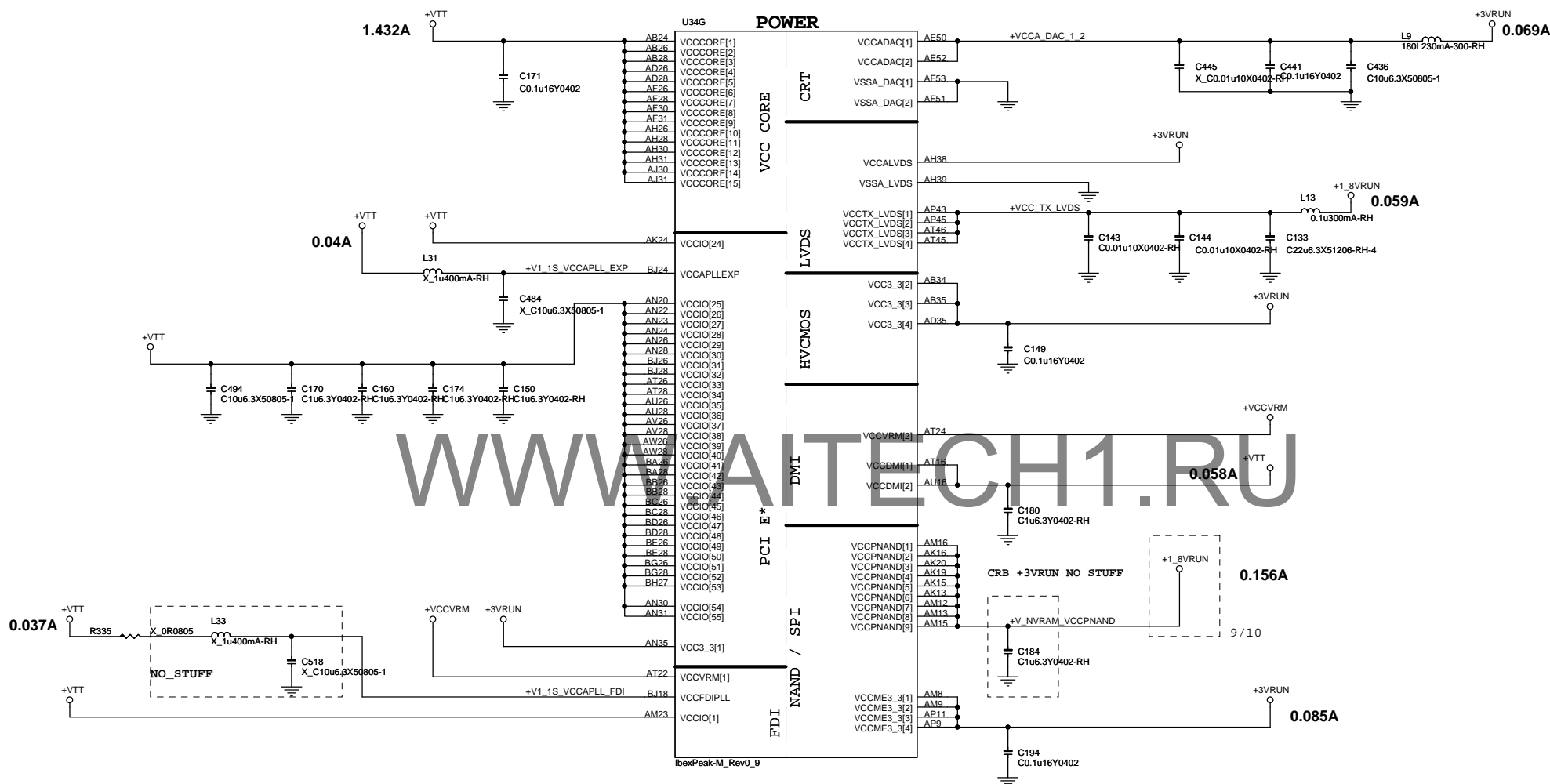
Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

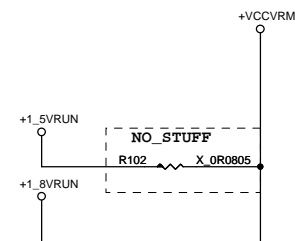


IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)

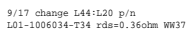



IBEXPEAK - M (POWER)

The VCCVRM rail (1.8 v/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAclk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.

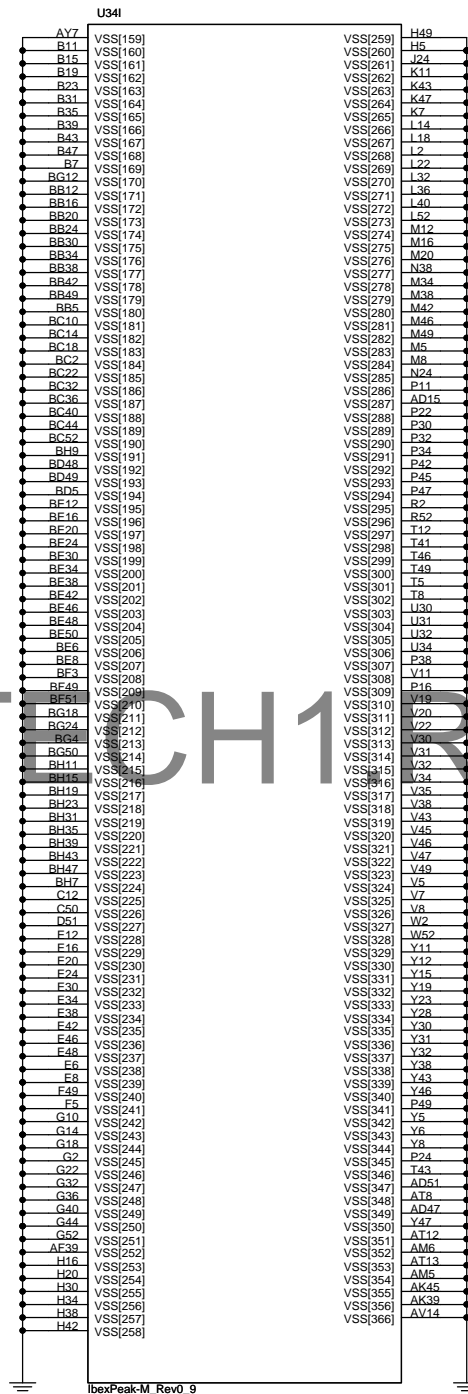


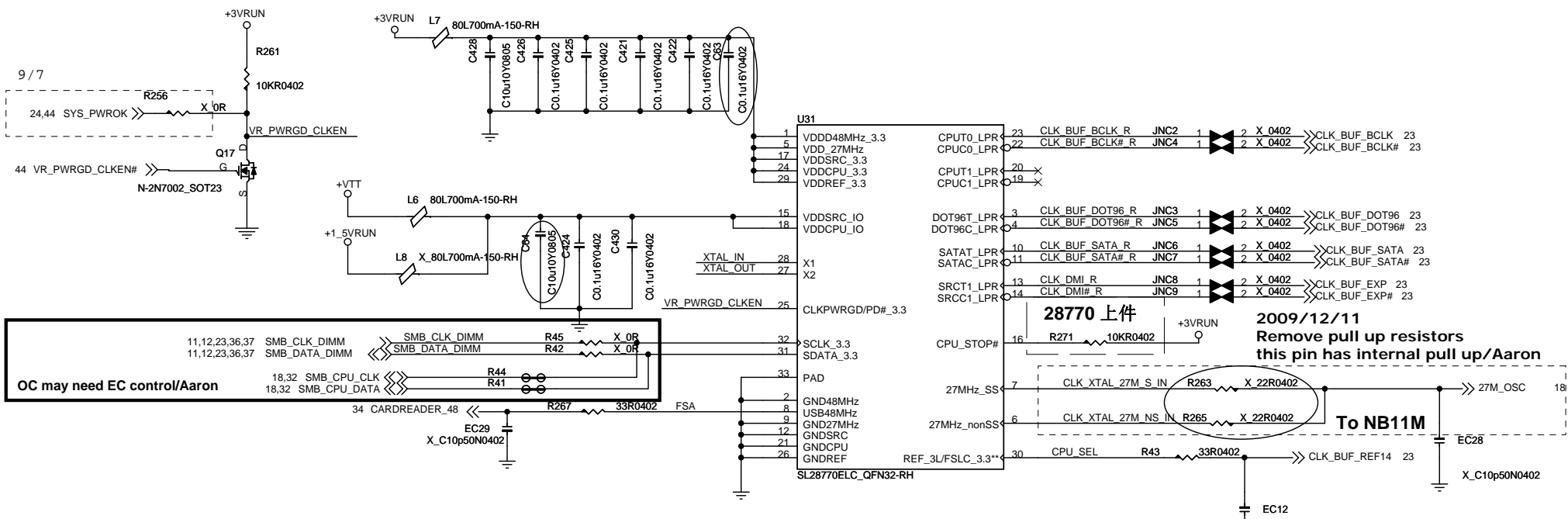
IBEXPEAK - M (POWER)



		MICRO-STAR INT'L CO.,LTD.	
Title			
IBEXPEAK - M (POWER)			
Size	Document Number	Rev	
Custom	MS-168A	()	
Date:	Friday, March 26, 2010	Sheet	29 of 52

VIEW.AIT CH1 RU

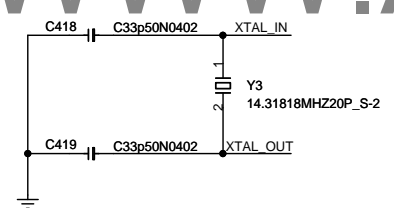




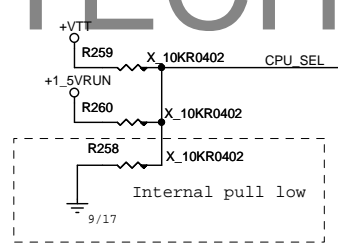
OC may need EC control/Aaron

28770 上件
2009/12/11
Remove pull up resistors
this pin has internal pull up/Aaron

Capacity select
If LC=20pf C708/C709=33pf
If LC=32pf C708/C709=56pf



For CPU frequency select (133MHz)



CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

2009/09/07 Reserved for 0A test
R346 is for Spread clock(Default use)
R347 is for non-Spread clock

Co-Lay Note:

For IDT IC9IRS3199
R84,R73,R71=10Kohm

For Silago SLG8SP587
R84,R73,R600=4.7Kohm

Note: add 0.1u cap at each power pin of LAN, please don't save.

Use External 1.05V Supply When Disable Switch Regulator.
If Using External 1.2V Supply Pls. Contact With FAE.

For RTL8105E
C3 to C6 are for VDD10 pins-- 3, 13, 29, 45.
For RTL8111E
C3 to C9 are for VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.

Need to modify L1 P/N to 2.2uH.

Pls. refer to
8111E Layout
Guide for L1,
C1, C2
selection
criteria.

Remove For Disable Switch Regulator
(Accept External 1.05V Power Supply)

C3 to C9 Close To
LAN chip

C11,C12 Close To LAN chip Pin 21.
C433* C11, C12 are for EVDD10 pins--21.

VDD33 power on rise time >1ms
C14 to C19 Close To LAN chip

Remove For Disable
Switch Regulator

Close to Transformer

LAN MAGNETICS

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R26 close to PIN46

R308

2.49KR1%0402

VDD33

AVDD33

MDIO+

MDIO-

VDD10

MDI1+

MDI1-

MDI2+

MDI2-

MDI3+

MDI3-

MDI4+

MDI4-

MDI5+

MDI5-

MDI6+

MDI6-

MDI7+

MDI7-

MDI8+

MDI8-

MDI9+

MDI9-

MDI10+

MDI10-

MDI11+

MDI11-

MDI12+

MDI12-

MDI13+

MDI13-

MDI14+

MDI14-

MDI15+

MDI15-

MDI16+

MDI16-

MDI17+

MDI17-

MDI18+

MDI18-

MDI19+

MDI19-

MDI20+

MDI20-

MDI21+

MDI21-

MDI22+

MDI22-

MDI23+

MDI23-

MDI24+

MDI24-

MDI25+

MDI25-

MDI26+

MDI26-

MDI27+

MDI27-

MDI28+

MDI28-

MDI29+

MDI29-

MDI30+

MDI30-

MDI31+

MDI31-

MDI32+

MDI32-

MDI33+

MDI33-

MDI34+

MDI34-

MDI35+

MDI35-

MDI36+

MDI36-

C461
C27p50N
C0402
C463
C27p50N
C0402
XTAL2
Y6
25MHz220P_S-2
XTAL1

VDD33
H For Enable Switch Regulator.
L For Disable Switch Regulator.
R68
R74 X_0R0402

EECS/SCL R66 10KR0402

REGOUT

AVDD33_REG

VDDREG

VDDREG

ENSWREG

EEDI/SDA

LED3/EEDO

EECS/SCL

DVDD10

LANWAKEB

DVDD33

ISOLATEB

PERSTB

LAN_RSTB

24,36,37

R277 1KR0402

R276 15KR0402

VDD33

CLK_GLAN_OE# R275 10KR0402

PCIE_WAKE# R285 10KR0402

10K ohm close to Host side

Close to LAN

PCIE_GLAN_RXN C1 C431 C0.1u10X0402

PCIE_GLAN_RXP C C432 C0.1u10X0402

PCIE_GLAN_RXN 23

PCIE_GLAN_RXP 23

CLK_PCIE_LAN# 23

CLK_PCIE_LAN 23

VDD33

EECS/SCL

LED1/EEPROM

LED2/EEPROM

LED3/EEDO

CS

VCC

NC

SK

DI

DO

GND

U10

EEPROM

R310 1KR0402

56/66

R273 X_10KR0402

R280 10KR0402

46

VDD33

GND

GND

GND

GND

GND

GND

GND

GND

GND

GND

GND

GND

GND

GND

GND

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GND

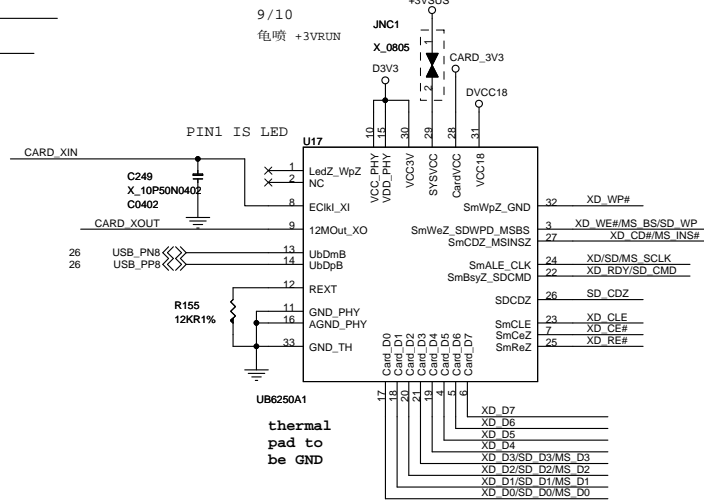
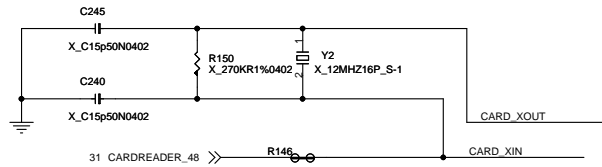
GND

MICRO-STAR INT'L CO.,LTD.

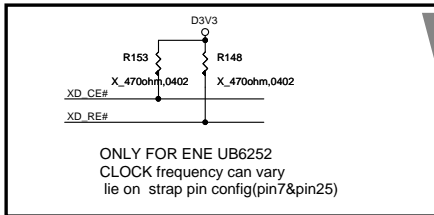
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Size C Document Number MS-168A

Date: Friday, March 26, 2010 Sheet 33 of 52

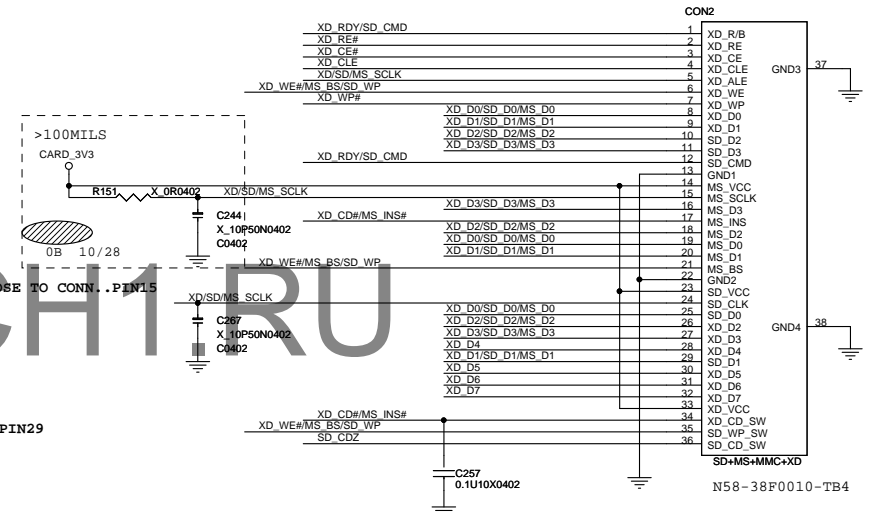
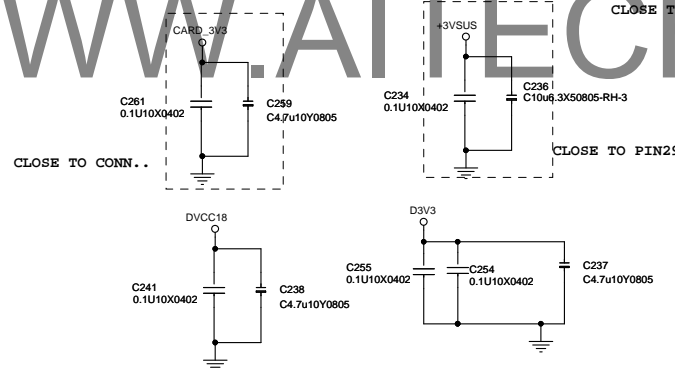


ENE UB6250 USB20 Flash Card Reader Controller						
Pins for SD, MMC, MS, and xD memory cards						
Name	No	I/O	XD	SD	MMC	MS
xDCeZ	7	O	xD card EN			
xDClE	23	O	xD CMD latch EN			
xDAlE	24	O	xD ADDR latch EN	SD clock	MMC clock	MS serial clock
xDByZ	22	B	xD Ready/busy	SD CMD/response	MMC CMD/response	
xDData0	17	B	xD D0	SD D0	MMC D0	MS D0
xDData1	18	B	xD D1	SD D1	MMC D1	MS D1
xDData2	20	B	xD D2	SD D2	MMC D2	MS D2
xDData3	21	B	xD D3	SD D3	MMC D3	MS D3
xDData4	19	B	xD D4		MMC D4	MS D4
xDData5	4	B	xD D5		MMC D5	MS D5
xDData6	6	B	xD D6		MMC D6	MS D6
xDData7	6	B	xD D7		MMC D7	MS D7
xDWeZ	3	B	xD W EN	SD WP		MS Busy
xDReZ	25	O	xD R EN			
xDWpZ	32	O	xD WP			
SDCdZ	26	I		SD CD	MMC CD	
xDcZ	27	I	xD CD			MS CD

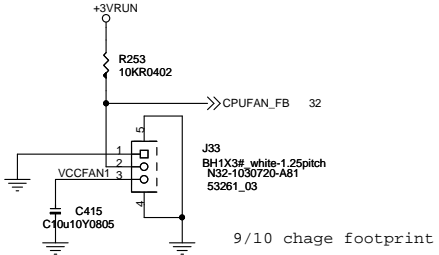
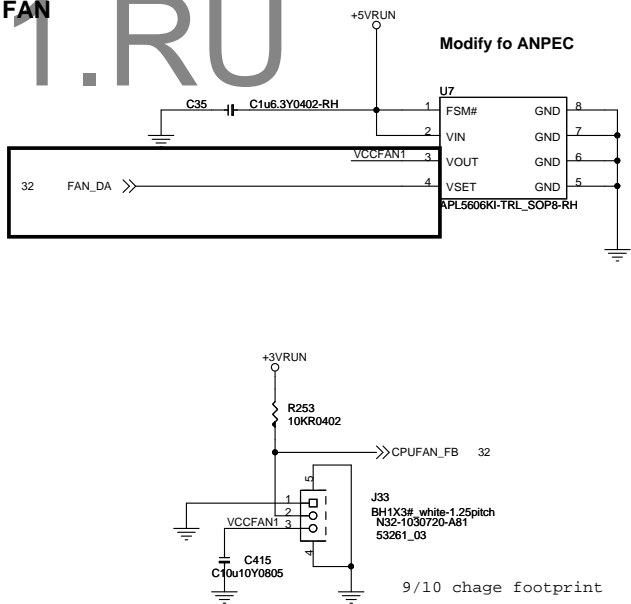
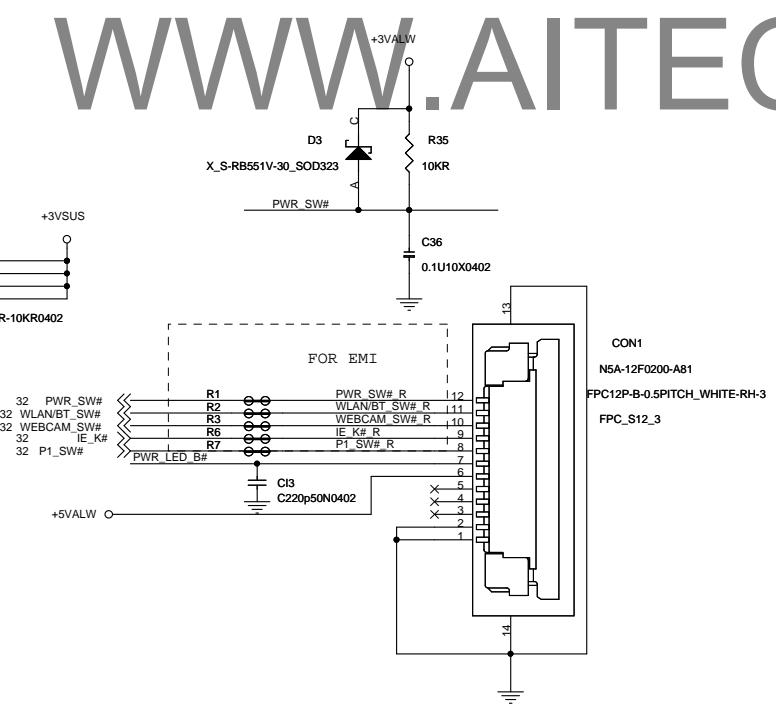
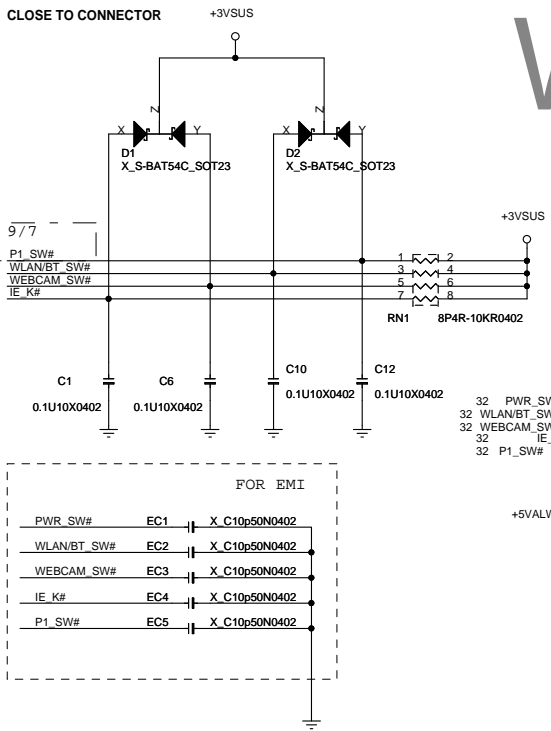
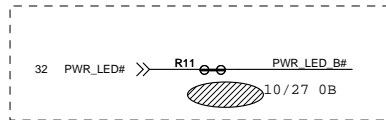
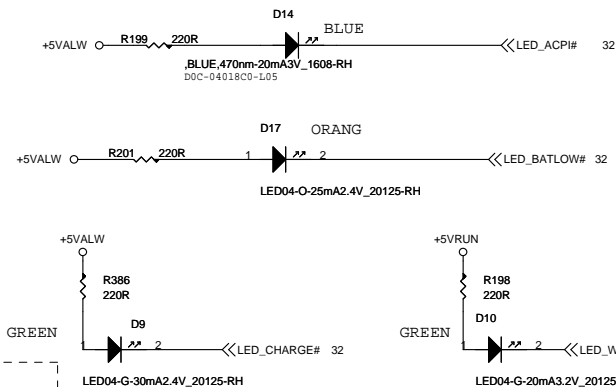
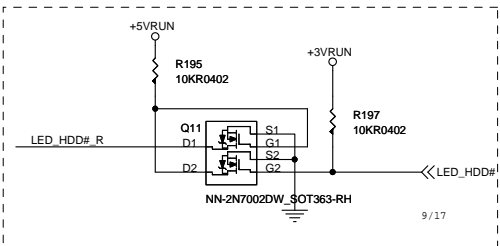
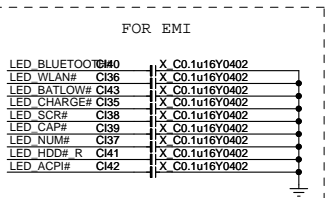
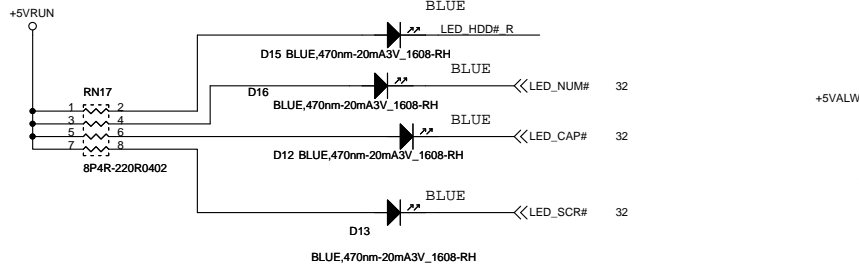


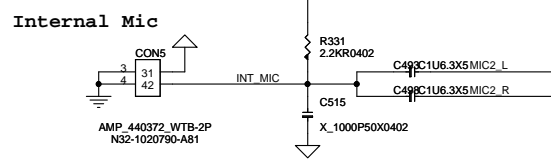
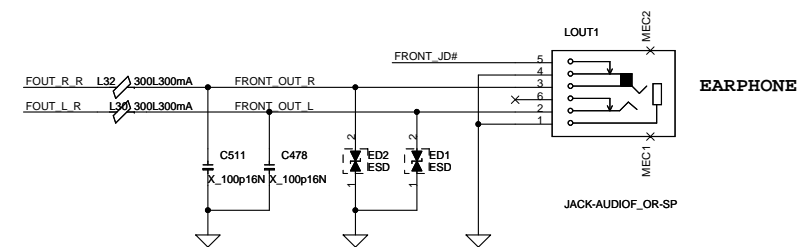
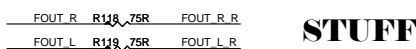
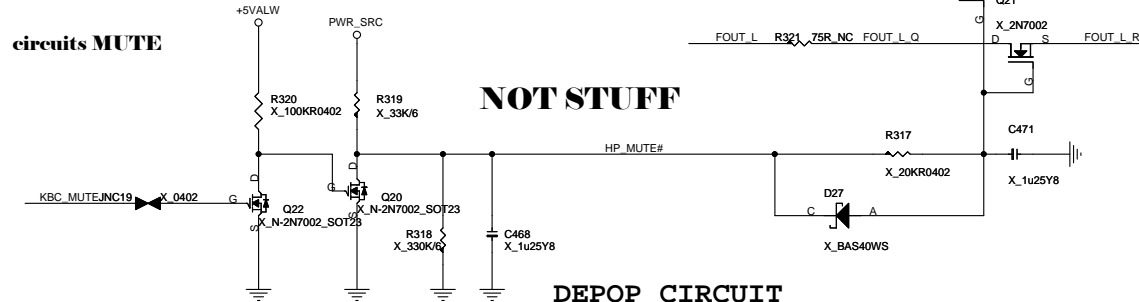
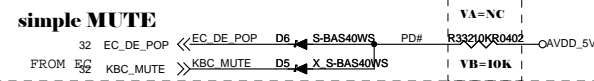
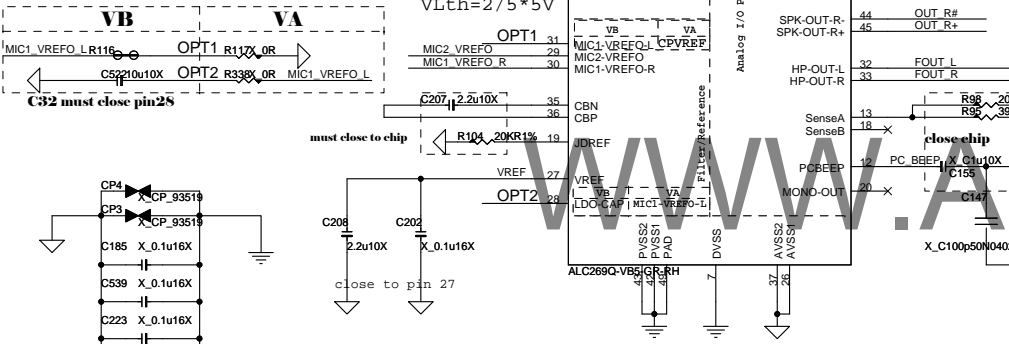
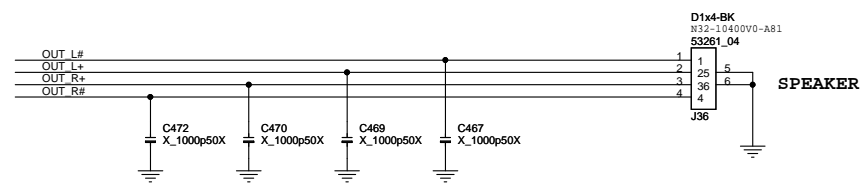
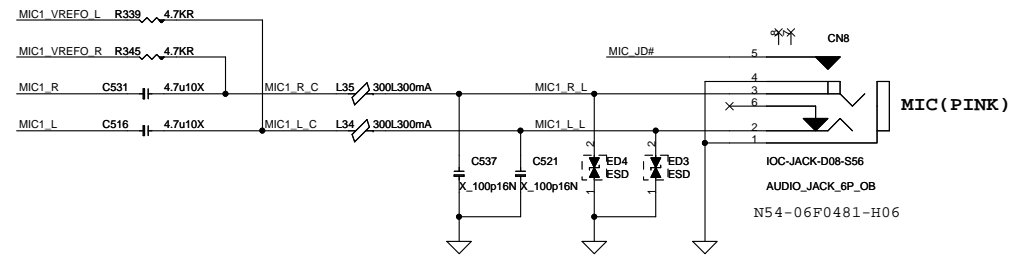
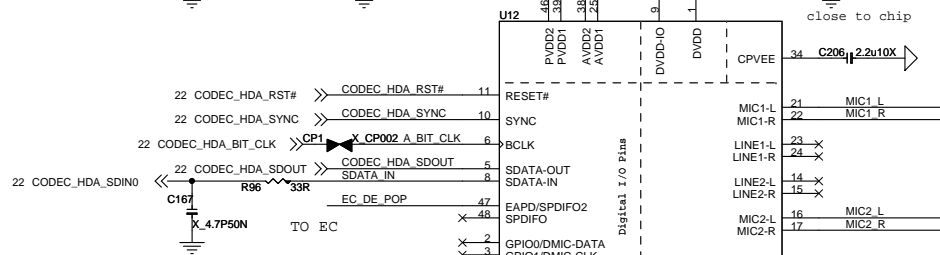
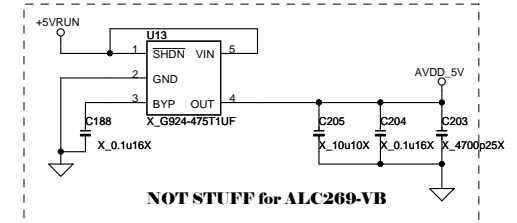
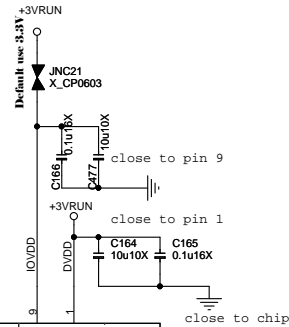
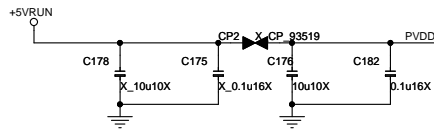
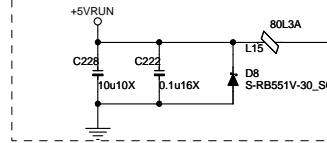
Configurations for Clock Source Selection:

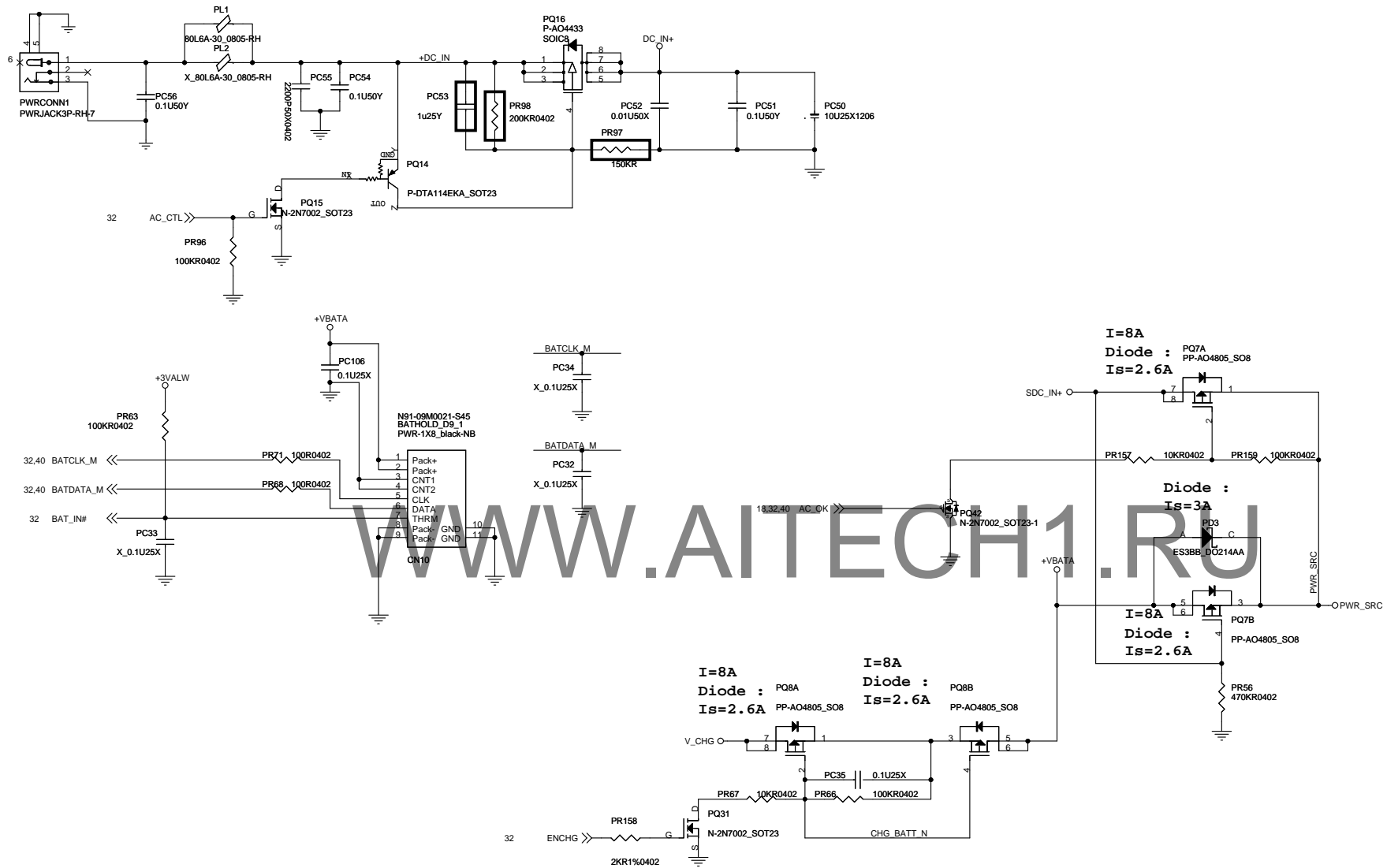
4.7K Pull-high Resistor on		Frequency of external clock source to EClin pin
xDReZ	xDCEZ	
NC	NC	48MHz
NC	O	24MHz
O	NC	12MHz

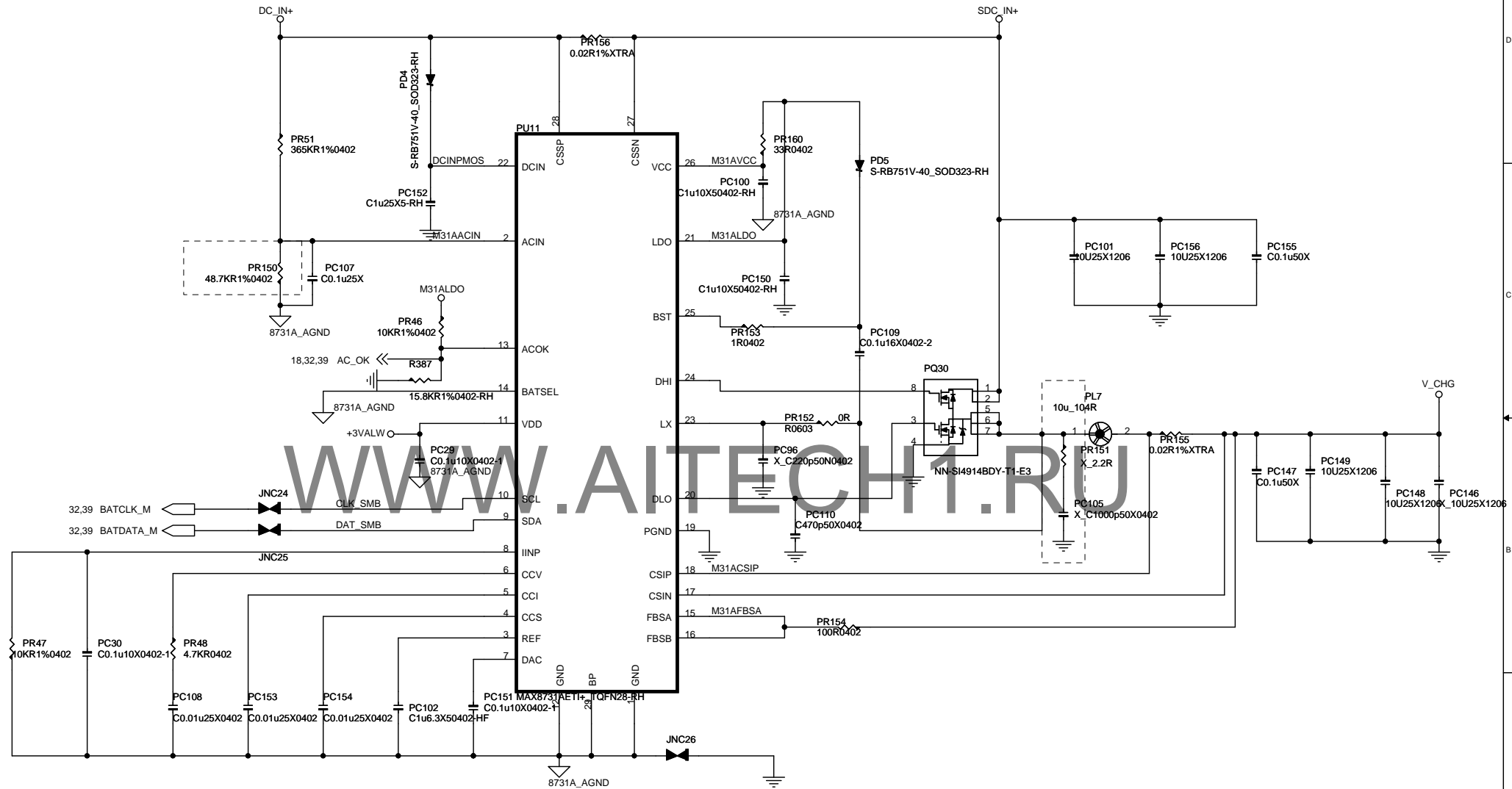


MICRO-STAR INT'L CO.,LTD.	
Title	Cardreader(UB6250)
Size	Document Number
Custom	MS-168A
Date:	Sheet 34 of 52









1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. $V_{IINP} = IINP_{UT} \times RS1 \times 3mA/V \times PR25$

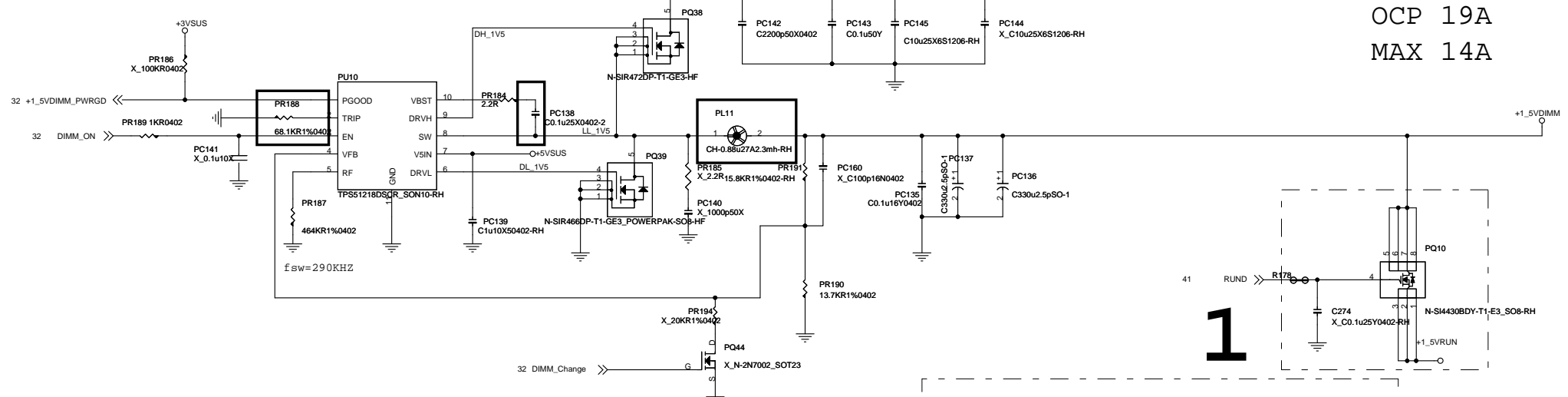
MICRO-STAR INT'L CO.,LTD.

Battery Charger

Size B	Document Number MC-100A	Rev 0A
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MS-168A

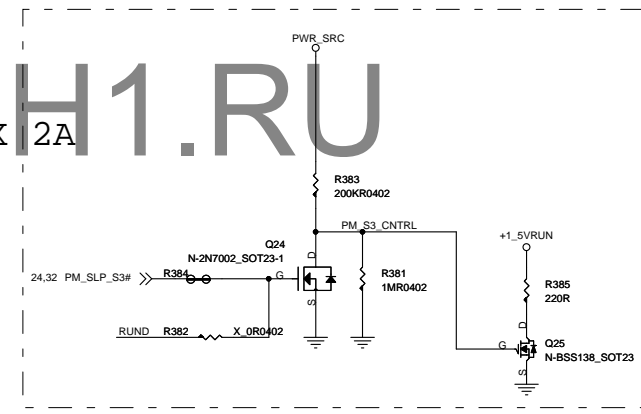
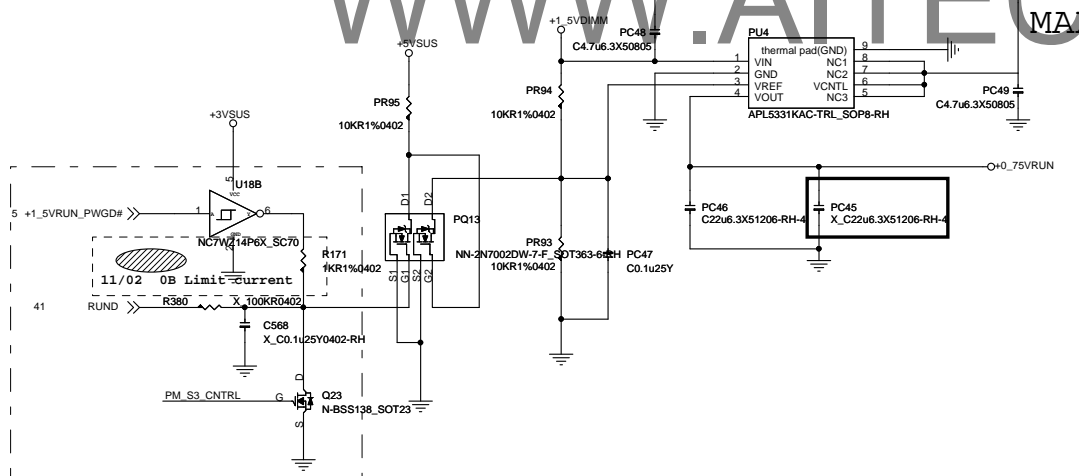
Date:	Friday, March 26, 2010	Sheet	40	of	52
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OCP 19A
MAX 14A

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MAX 2A

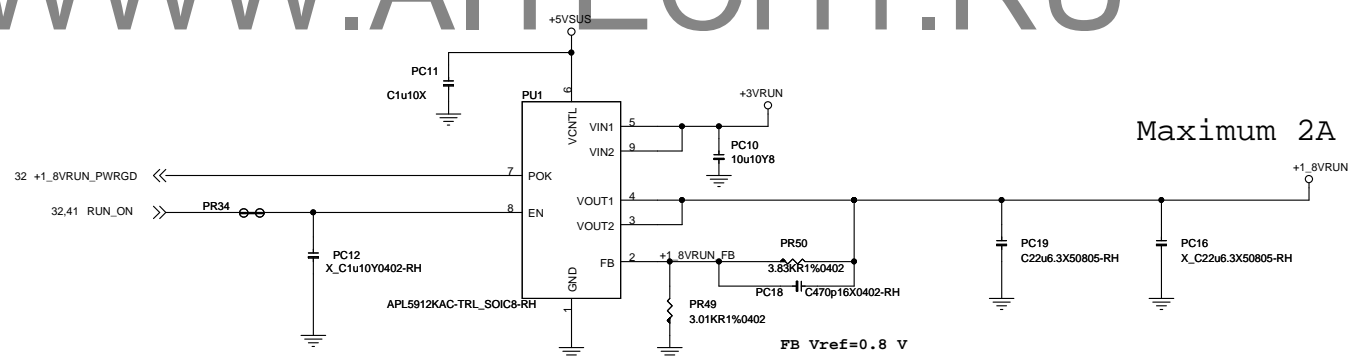
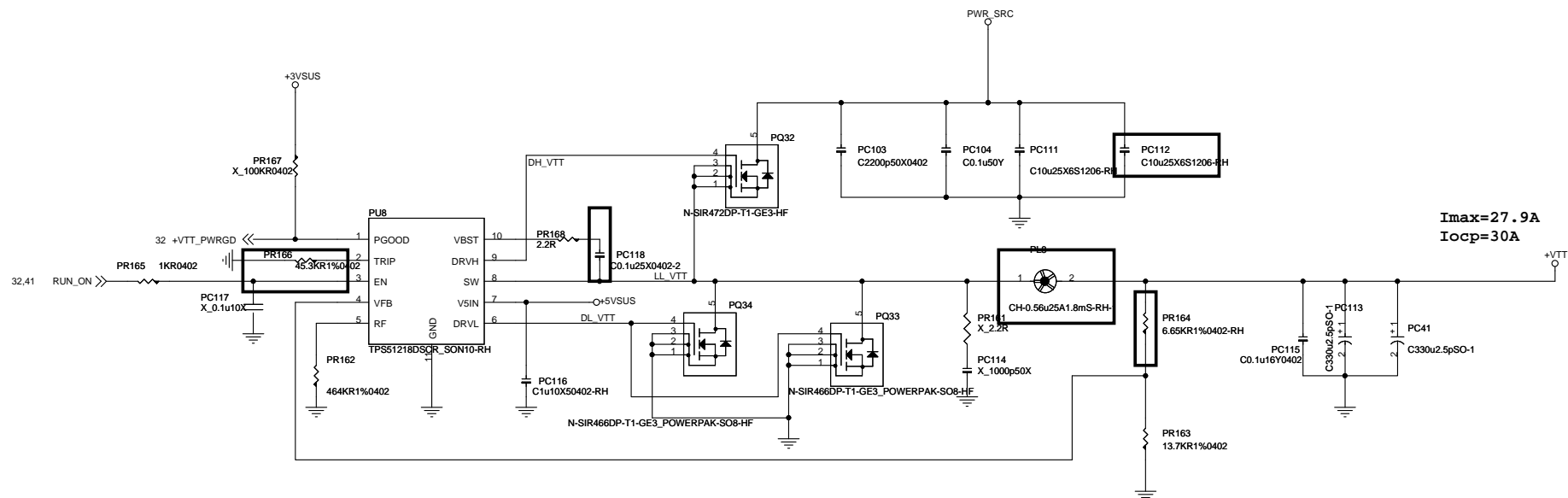



8

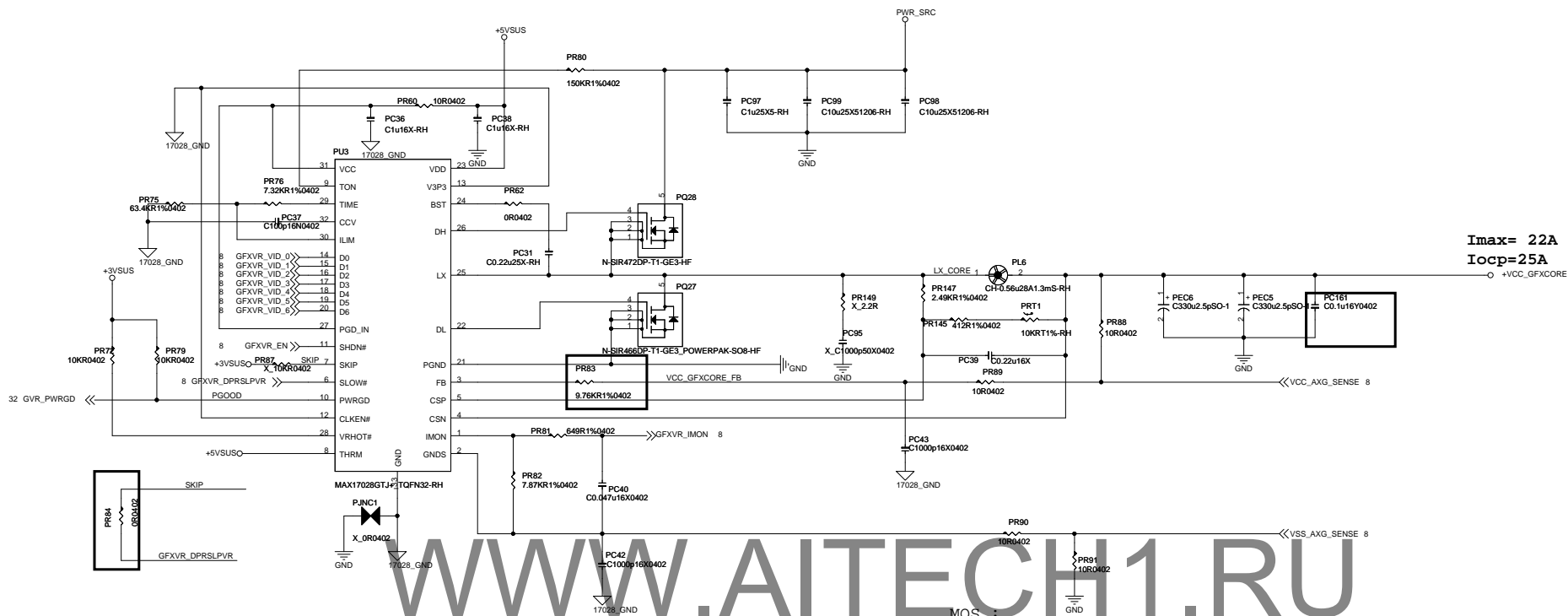
1

2

MICRO-STAR INT'L CO.,LTD.			
Title	SMDDR VTERM /1 5VRUN		
Size	Document Number	Rev	
Custom	MS-168A	0A	
Date:	Friday, March 26, 2010	Sheet	42 of 52

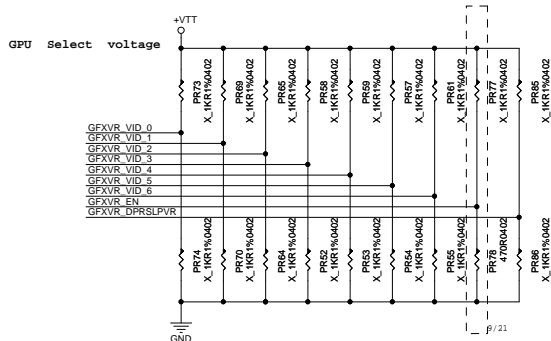
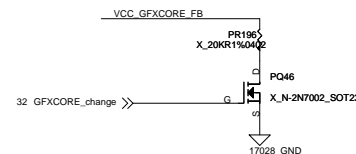


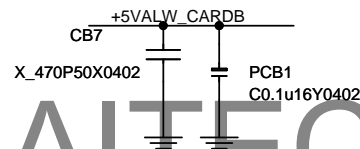
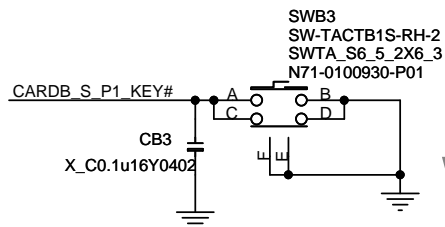
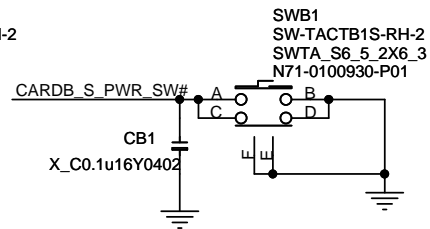
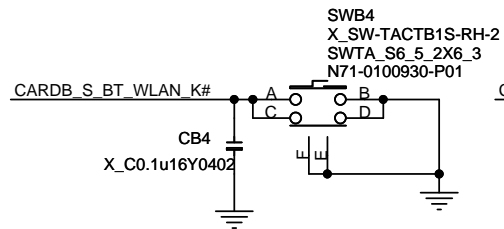
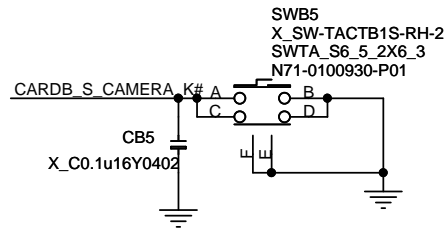
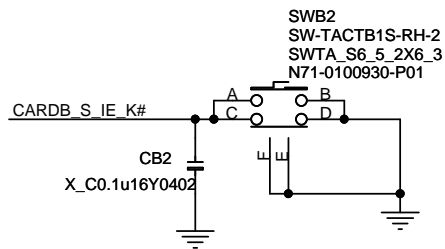
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Title VTT Power,+1.8VRUN			
Size Custom	Document Number MS-168A	Rev 0A	
Date: Friday, March 26, 2010		Sheet 43	of 52



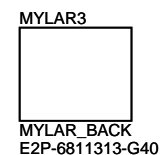
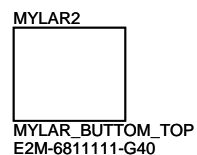
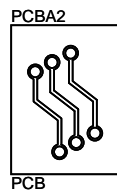
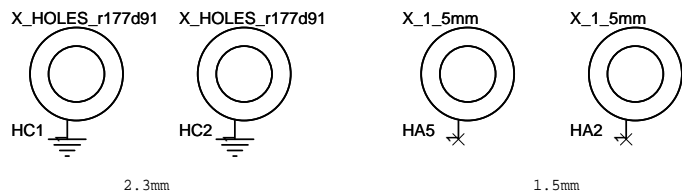
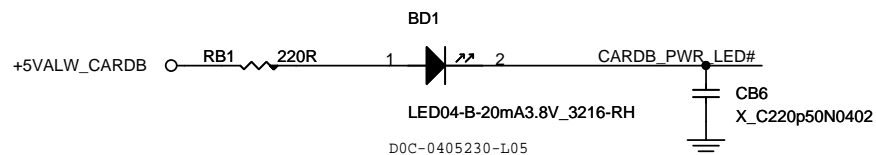
Imax= 22A
Iocp=25A
+VCC GFXCORE

MOS :
high side : main : D03-L142600-A68
 seond : D03-1200300-I14
low side : main : D03-L141200-A68
 seond : D03-42N0330-I14





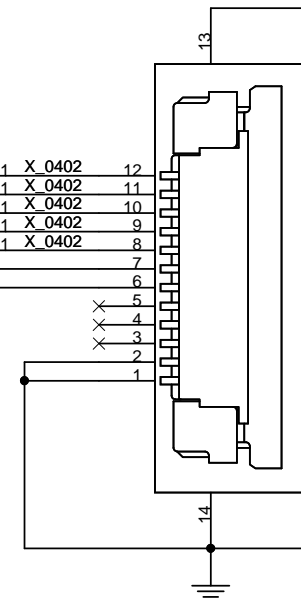
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P30-168AB10-D05
P30-168AB10-H73

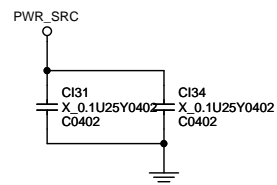
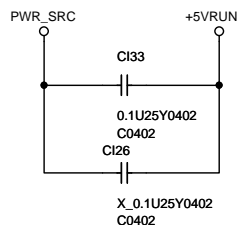
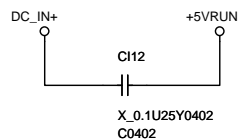
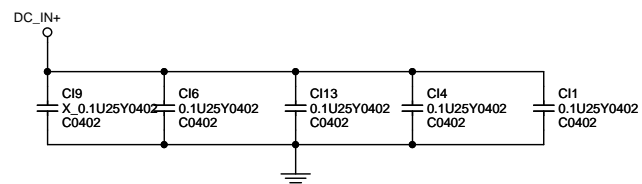
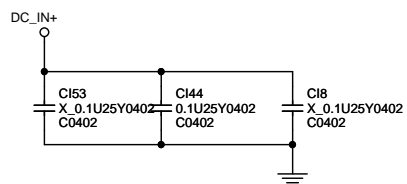
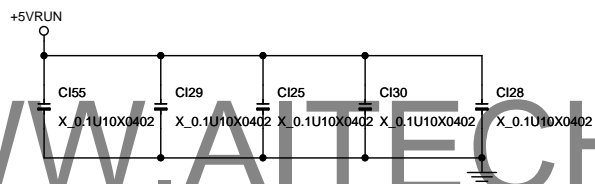
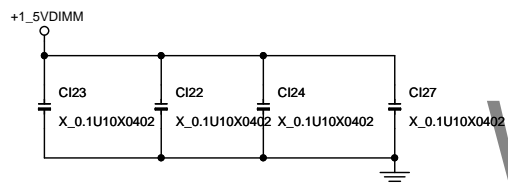
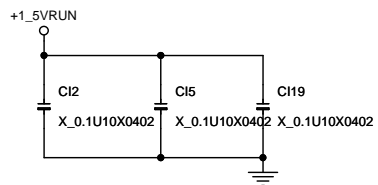
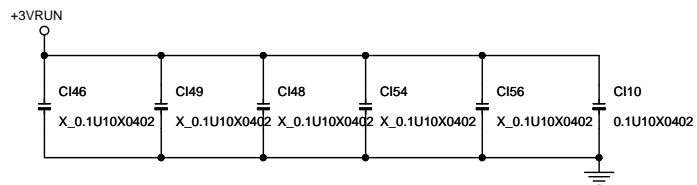
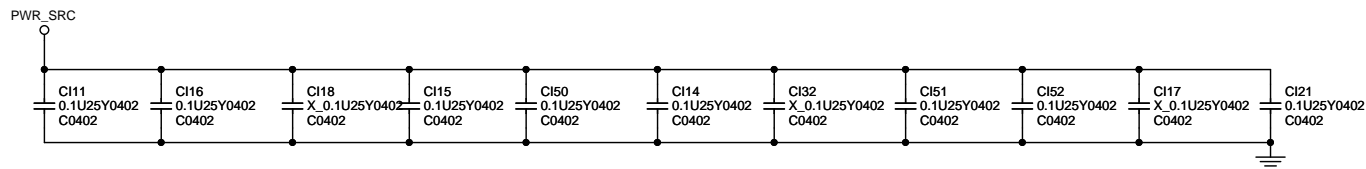
CARD_B_ BUTTOM

CARDB_S PWR SW#	JNCB1	2	1	X_0402	12
CARDB_S BT WLAN K#	JNCB4	2	1	X_0402	11
CARDB_S CAMERA K#	JNCB5	2	1	X_0402	10
CARDB_S IE K#	JNCB2	2	1	X_0402	9
CARDB_S P1 KEY#	JNCB3	2	1	X_0402	8
CARDB_PWR_LED#					7
+5VALW_CARDB					6
					5
					4
					3
					2
					1



FPC2
FPC12P-B-0.5PITCH_WHITE-RH-3
N5A-12F0200-A81
FPC_S12_3

MICRO-STAR INT'L CO.,LTD.		
Title Lauch Board B		
Size Custom	Document Number MS-168A	Rev 0A
Date: Friday, March 26, 2010	Sheet 49	of 52



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Title		MICRO-STAR INT'L CO.,LTD.	
Size		EMI	
B		Document Number	
Date:		MS-168A	
Friday, March 26, 2010		Sheet 50 of 52	
Rev		0A	

0B
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MSI CORPORATION			
Title Change Histoy			
Size Custom	Document Number MS-168A		Rev 0A
Date:	Tuesday, January 05, 2010	Sheet 52 of 52	